Four types of control panel may be used for mounting:

- Full Control Panel
- Extended Control Panel
- Mini Panel
- Portable Panel.

FULL CONTROL PANEL

The Full Control Panel is the standard control panel for the P856M. It is 2U (88.90 mm) high.

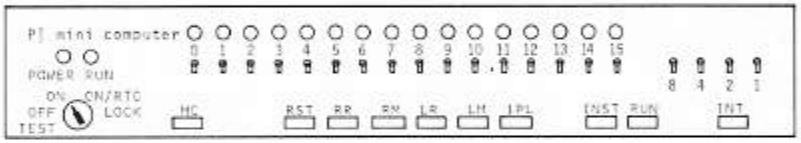

Figure 12.1 Full Control Panel

The facilities available on the full control panel are:

Safety Key Switch
A five position key operated switch providing the main on/off facility. The five positions are:

1. TEST - *Micro diagnostics*
In this position an elementary system test can be performed without any external tool. For a description of the microdiagnostics see page 14-7.

2. OFF - *Power off*

3. ON - *Power on*
In this position an elementary system test can be performed without any external tool. For a description of the microdiagnostics see page 14-7.

4. ON/RTC - *Power on/RTC on*
In this position the CPU is able to run with the Real Time Clock on. All the remaining control panel switches are effective.

5. LOCK – *Power on/RTC on*
In this position the CPU is in run mode with the Real Time Clock on. All the remaining control panel switches with the exception of the INT button are inhibited.

Display Lamps

1. Power Lamp
Situated above the Safety Key Switch, lit when the Safety Key Switch is in all but the Off position and power is being supplied to the system.

2. Run Lamp
Situated above the Safety Key Switch, lit when the CPU is operating in Run mode.

3. Data Lamps
Sixteen lamps situated one above each data switch and numbered 0 - 15. The lamps are lit to indicate the contents of the registers, memory, or status word depending on the settings of other control switches. A 1 bit is indicated where a lamp is lit.

Data Switches
Sixteen numbered data switches. Each switch is a two position switch used for loading the appropriate data bit into a register or memory, depending on the setting of other control switches. A 1 bit is loaded when a switch is in the up position.

Register Address Switches
Four switches mounted to the right of the data switches and used to code the address of the register to be used when reading or loading a register from the Data Switches. The switches are numbered with the address value they represent in binary (8, 4, 2, 1), giving an addressing capability of 0 - 15.

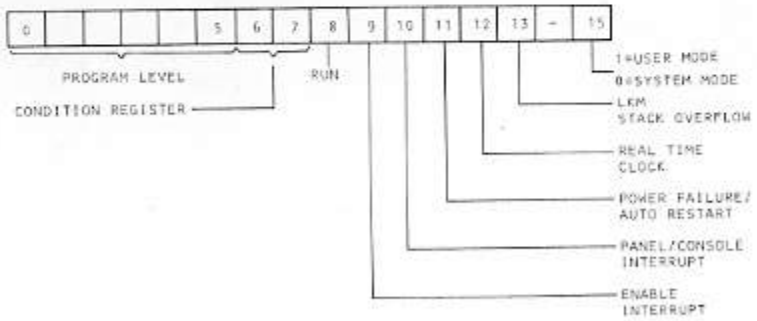

Figure 12.2 Display of status

Control Buttons
The five control buttons are situated nearly centrally beneath the Data Switches. Each button is spring loaded to return to its original position after being depressed and selects and initiates a specific function:

1. RST – *Read Status*
   Depressing this button causes the contents of Program Status Word register (Pl.CR.GF.) to be displayed on the lamps.

2. RR – *Read Register*
   Depressing this button causes the contents of the register addressed by the Register Address Switches to be displayed on the Data Lamps.

3. RM – *Read Memory*
   Depressing this button causes the contents of the memory location addressed from the contents of the P Register to be displayed on the Data Lamps. The contents of the P Register are also incremented by 2.

4. LR – *Load Register*
   Depressing this button causes the value set on the sixteen Data Switches to be loaded into the register addressed by the Register Address Switches. The value is also displayed on the Data Lamps.

5. LM – *Load Memory*
   Depressing this button causes the value set on the sixteen Data Switches to be loaded into the memory location addressed from the contents of the P Register. The value is also displayed on the Data Lamps and the contents of the P Register are incremented by 2.

Mode Buttons
The two mode buttons are situated beneath Data Switches 14 and 15. They select and initiate the following modes of operation.

1. INST – *Single Instruction Mode*
   Depressing this button causes the CPU to execute the instruction addressed from the contents of the P Register, and then stop.

2. RUN – *Run Mode*
   Depressing this button causes the CPU to execute the instructions of a program as directed by the program and commencing at the instruction addressed from the contents of the P Register.

Service Buttons
There are three service buttons:

1. MC – *Master Clear*
   Situated beneath Data Switch 0
   Depressing this button raises the master clear level throughout the system whilst it is depressed, causing a general reset of all the associated logic.

2. INT – *Interrupt*
   Situated beneath the Register Address Switches.
   Depressing this button raises a control panel interrupt.
   This button is the only control operative when the Safety Key Switch is in the LOCK position.

3. IPL – *Initial Program Loader*
   Situated beneath Data Switch 10.
   This button will only be present if the IPL option is fitted. In such cases, when the button is depressed it causes the Initial Program Loader to be loaded into central memory and the cpu to be started. Loading is carried out from the device and via the channel specified by the setting of the sixteen Data Switches.

TRANSPORTABLE PANEL

This panel is a free standing full control panel. It is fitted with a connector to enable it to be connected in place of a fixed full control panel or minipanel for mainly servicing purposes.

MINIPANEL

The minipanel may be fitted, on option, to replace the full panel and offers the following facilities:

1. Safety Key Switch
2. Interrupt and Start Buttons
3. Power and Run Indicators.

EXTENDED CONTROL PANEL

The Extended Control Panel is a 4U (177.80 mm) high panel which may be mounted when the CPU is plugged into the 10-slot M4 or M4M box or the 17-slot M5M mounting box (standard for P857M).
This panel permits to have an address and its contents displayed at the same time. Moreover the panel allows debugging facilities as processing may be stopped at any address set previously on the upper row of switches. The user may then load new data.
Addressing from this panel is word oriented.

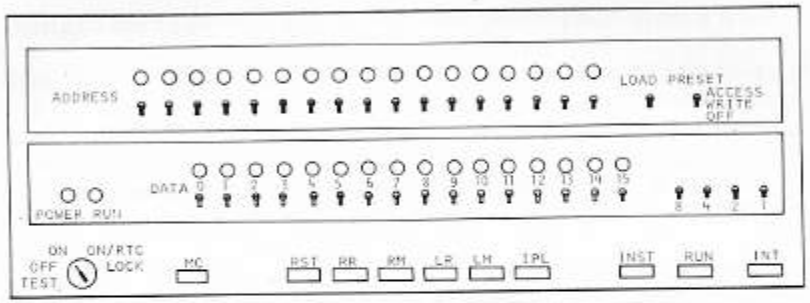

Figure 12.3 Extended Control Panel

The functions of the switches and displays are:

Display lamps
Seventeen lamps situated one above seventeen address switches. When the computer is running the lamps are lit to indicate addresses on the upper part of the panel and data on the display lamps of the lower part. When the CPU stops the contents of the next instruction's address is displayed on the lower part and the address of the instruction on the upper part.

Address switches
Seventeen address switches on the upper part of the panel. Each switch is a two position switch used for loading the appropriate address pattern. A 1 bit is loaded when a switch is in the 'up' position.

LOAD spring-loaded switch
Used to load an address in an address register contained in the control panel. The required address is set on the address switches. The LOAD switch is pressed downwards and the address is displayed on the address lamps.

PRESET switch
A three position switch for debugging purposes:

ACCESS - *stop on memory access*
In this position the CPU stops when a physical address generated by the CPU is identical to the pattern coded on the address keys. If the address is detected the relating instruction is executed and the CPU goes in the idle state.

WRITE - *stop when writing into memory*
In this position the CPU only stops if a store operation is performed in the location whose address was set previously on the address keys.

OFF
The switch is set in this position when debugging is not required.

Reading and loading memory is realised by using the RM and LM buttons. The instruction counter P remains unaffected during these operations as only the address register in the control panel is incremented. It is therefore not necessary to reload P before restarting the program.
The use of the RM and LM buttons is slightly different when the Extended Control Panel is used compared to the description under Full Control Panel.

Read Memory Procedure
- First load the address register with the required address (see LOAD addr).
- Press RM button. The contents of the memory location is displayed on the data lamps.
- The control panel register is incremented by two and the next address is displayed on the address lamps.
  Each time the RM button is pressed the address register is incremented and the contents of the next memory location appears on the data lamps.

Load Memory Procedure
- First load the address register with the address required (see LOAD addr).
- Set the value to be loaded on the data switches.
- Press LM button.
  The value is displayed on the data lamps. The address register is incremented and displayed on the address lamps.

All other pushbuttons and switches have the same meaning as described under FULL CONTROL PANEL.

The basic loading and operating facilities are all carried out at the CPU control panel by the use of the control panel switches. Facilities exist at the panel to enable an operator to load and display selected memory locations and registers, to start the CPU, and to raise a control panel interrupt. In addition an optional facility is available to enable the direct loading of an Initial Program Loader, or similarly written program, from various devices.

PROGRAM LOADING

Program loading may be carried out in 4 separate stages:

1. LOAD BOOTSTRAP - (MACHINE CODE)
2. LOAD INITIAL PROGRAM LOADER - (MACHINE CODE)
3. LOAD SYSTEM OR USER PROGRAM - (OBJECT CODE)
4. LOAD USER PROGRAM - (OBJECT CODE)

Bootstrap
This program is a basic program used to load more sophisticated loader programs. The bootstrap will only load programs which are written in machine code (binary form) and will normally only carry out a checksum to determine errors.

Initial Program Loader
The programs which are classed as initial program loaders are able to load object code clusters into memory and may contain error reporting and other facilities required at the time of loading system or user programs. Initial Program Loaders are written in machine code (binary form) and are loaded using a bootstrap program.

System Programs
Certain of the system programs (monitors) have the facility to load user programs, in these cases the routines within the system program provide the same functions as the initial program loaders.

INITIAL PROGRAM LOADER

The initial program loader provides the system with the ability to automatically load and run an initial program loader, or similar program, from devices connected to the programmed or an input/output processor channel.

Organization
The option consists of a 64-word ROM mounted on the CPU card, and holding a bootstrap program, and the necessary control circuits to load and run the bootstrap using parameters previously set onto the 16 data switches. The parameters set on the data switches are:

bit

0 1 = IPL loaded from ASR, 4 × 4 format
0 = IPL loaded from other devices

1 1 = IPL loaded from disc
0 = IPL loaded from other devices

2 1 . Not used if bit 0 was 0

3 1 = Programmed Channel
0 = I/O Processor

4 - 7 control information for control unit
TY = 0001 MT = 0010
TK = 0111 DK = 0011

8 1 = multiple device control unit
0 = single device control unit

9 1 if disc in system is used

10 - 15device address of device from which IPL is loaded

Where a device has no specific setting requirements on the data switches, for example Cassette Tape, it is sufficient to set the switches to define; 'Other Devices', the correct channel, and the device address and qualification required for the CIO start command.

Operation
The operation of the initial program loader consists of 4 main steps:

1. The bootstrap is copied from the ROM into the first 64 words of central memory.
2. The contents of the 16 data switches are copied into register A15.
3. The CPU is put into INHIBIT INTERRUPT state.
4. The P register is loaded with zero and the CPU started in run mode.

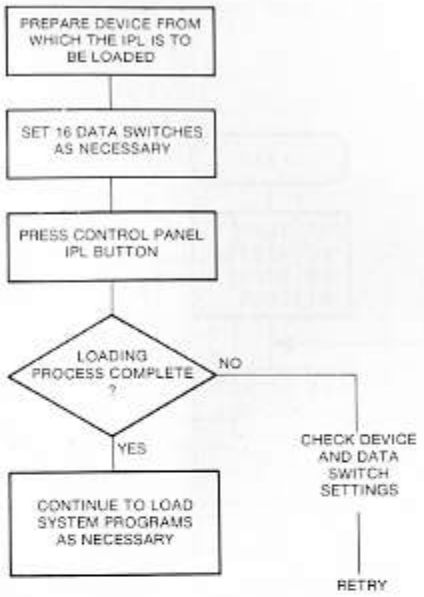

Figure 13.1 Loading the IPL

LOAD MEMORY (FULL CONTROL PANEL)

Figure 13.2 shows the procedure for loading data into memory.

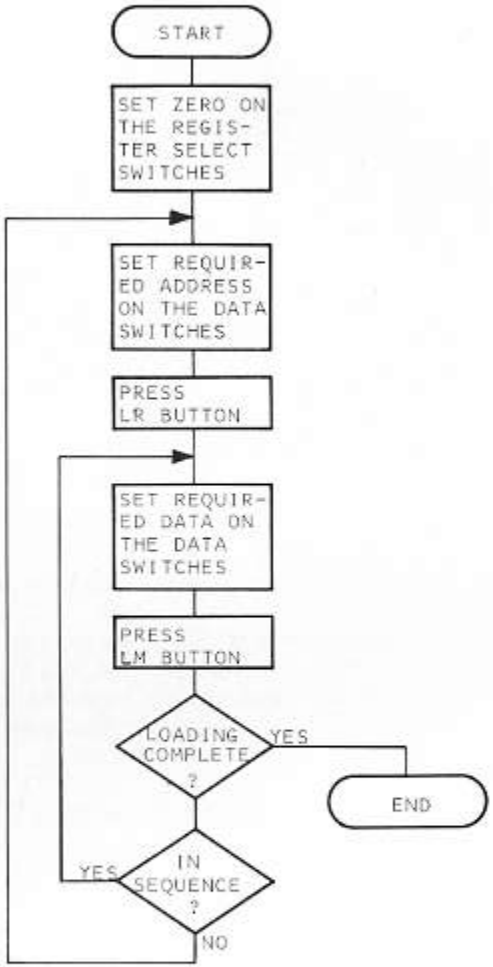

Figure 13.2 Loading Data into Memory

LOAD MEMORY (EXTENDED CONTROL PANEL)

Figure 13.3 shows the procedure for loading data into memory.

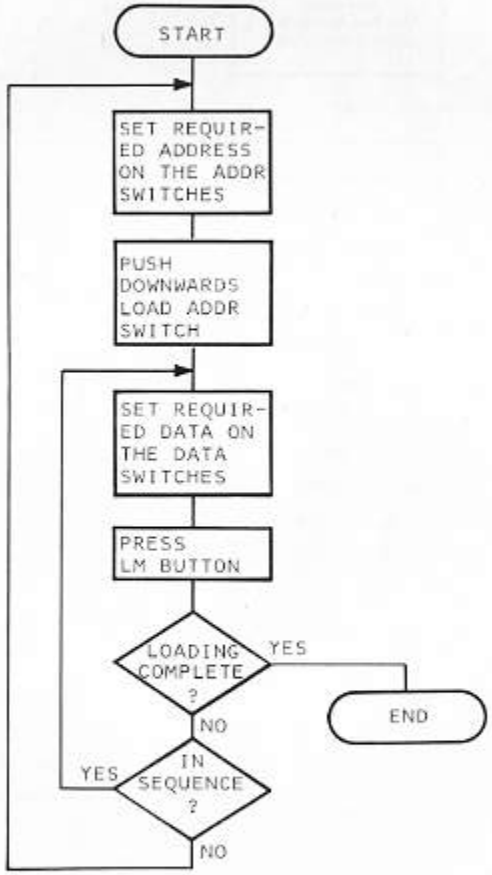

Figure 13.3 Loading Data into Memory

READ MEMORY (FULL CONTROL PANEL)

Figure 13.4 shows the procedure for displaying the contents of memory.

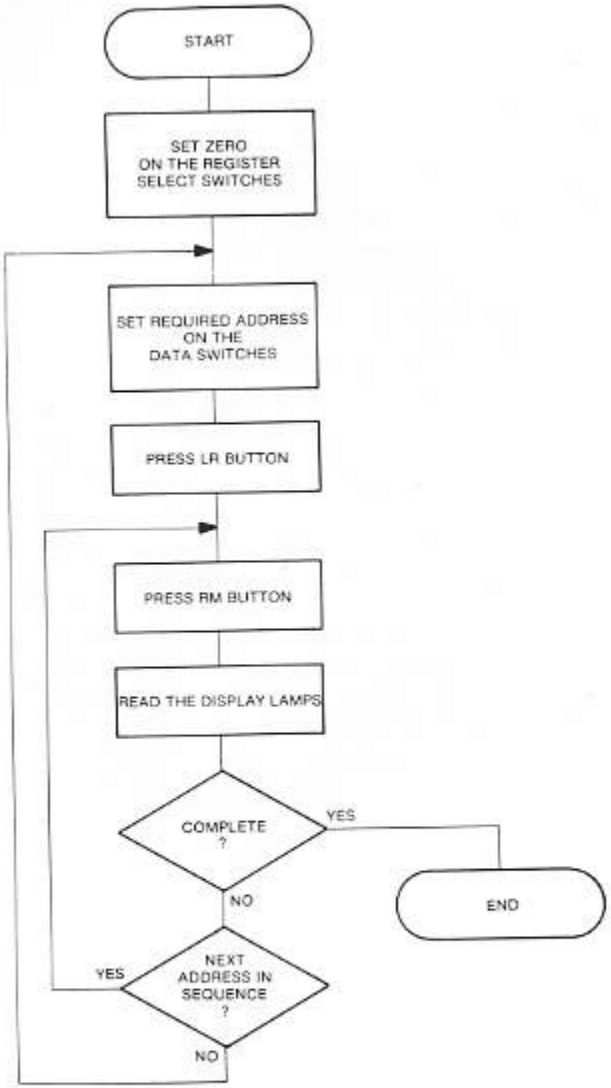

Figure 13.4 Displaying Memory Contents

READ MEMORY (EXTENDED CONTROL PANEL)

Figure 13.5 shows the procedure for displaying the contents of memory.

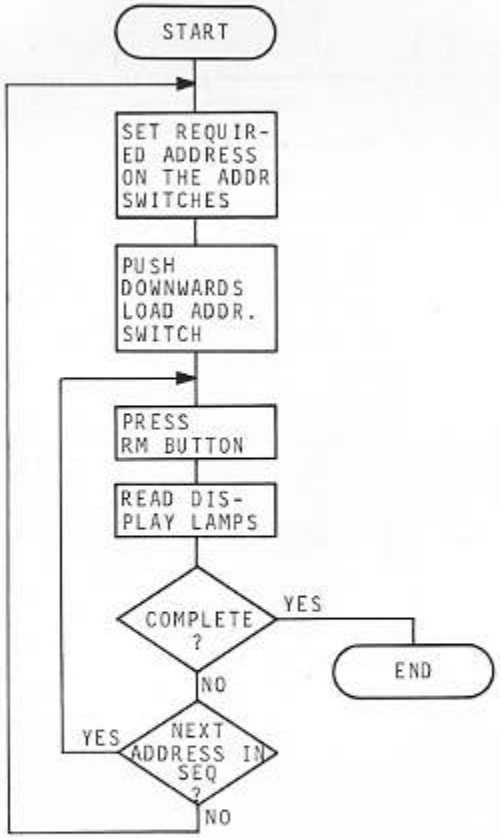

Figure 13.5 Displaying Memory Contents

LOAD REGISTER

Figure 13.6 shows the procedure for loading data into one of the 16 general purpose registers.

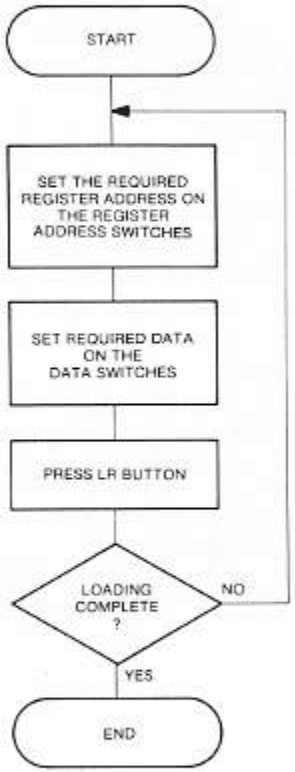

Figure 13.6 Loading Data into Register

READ REGISTER

Figure 13.7 shows the procedure for displaying the contents of one of the 16 general purpose registers. The contents of the program status word may be displayed by pressing the RST button.

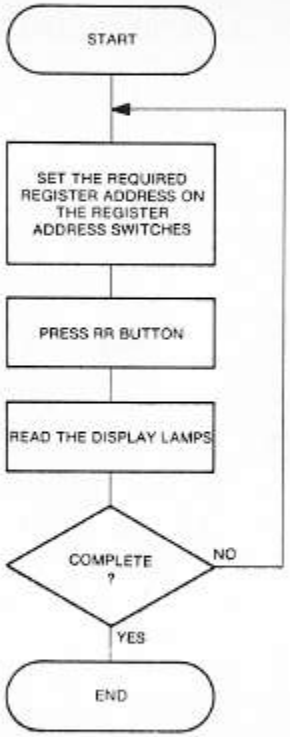

Figure 13.7 Displaying Register Contents

Apart from the main facilities already covered the following additional features are:

1. POWER FAILURE - AUTOMATIC RESTART
2. INTEGRATED V24/V28 SERIAL CONTROL UNIT
3. REAL TIME CLOCK
4. MICRODIAGNOSTICS
5. DETECTION OF PRIVILEGED INSTRUCTIONS

POWER FAILURE - AUTOMATIC RESTART

This facility provides the processor with the ability to terminate processing in an orderly manner after the detection of a power failure, and to restart and resume processing correctly after the restoration of power.

Apart from separate peripherals, all the system's power supplies, whether within the basic cabinet or equipment shelves, are considered necessary for the correct operation of the system. The failure of any of the supplies is therefore able to raise the power failure signal.

Operation

The power failure signal can be connected to any one of the 8 highest priority interrupt levels. When power failure is detected an interrupt is raised and input/output processor exchanges are inhibited, control of the general purpose bus being given to the CPU. Interrupt action takes place and the associated interrupt routine is executed to save the contents of registers, and if necessary specific areas of MOS memory. Core memory is already protected and thus no loss of data from core occurs even if total power failure occurs before completion of the saving routine. On restoration of power the system restarts and CPU operation continues with the restoration of all registers and areas saved before completing the interrupt routine and returning to the originally interrupted program. The power failure interrupt is reset as necessary by the use of the Reset Internal Interrupt (RIT) instruction.

The power failure signal may also be raised at initial power on time if the control panel key switch is set to the LOCK position. In this position the CPU is started and provided the power failure signal is connected to an interrupt level the restoring routine of the level is carried out to restart normal operation at the point it was last suspended.

When the power failure signal is not connected, the CPU will start and remain in the idle state at power on, or after restoration of power following a failure.

Limits
Power failure is set at least 2 ms before the voltage drops below the acceptable limit.

The saving routine should not last more than 2 ms.

Power failure is not set for detected losses of less than 5 ms. The contents of a memory location involved in a memory cycle at the time of total failure is not guaranteed.

REAL TIME CLOCK

A real time clock is available within the system, control of the clock being provided by the control panel key:

ON - RTC stopped
ON RTC - } RTC running
LOCK - }

Once running the RTC generates a signal with reference to the main power supply frequency and is not able to be stopped by program. The generated signal may be connected to any of the 8 highest priority interrupt levels and is thus able to raise an interrupt every 20 ms for 50 cps supplies or 16.67 ms for 60 cps supplies. The associated interrupt must be cleared using the Reset Internal Interrupt (RIT) instruction and the RTC routine may be used as required within the system.
An optional programmable real time clock is available on one board, requiring one slot in the mounting box.

INTEGRATED V24/V28 SERIAL CONTROL UNIT

A V24/V28 Serial Control Unit is available within the system mounted on the CPU board. This control unit allows to attach one of the following asynchronous peripherals as I/O console:

- ASR
- PER3100
- Display

} with V24 interface

The transmission speeds are 110, 600, 1200, 2400, 4800 or 9600 bps.
The speed selection is made by straps on the card. Also selected by straps may be the parity; odd, even or no parity. Odd or even parity is generated or checked by the controller. The number of stop bits, one or two, is also selectable by straps and are generated by the controller.

Organisation
Operation of the control unit is only possible via the programmed channel through the general purpose bus. Connection from the control unit to the peripheral must be according the V24/V28 recommendations.
Data are transferred serially to the control unit and is carried out in parallel by the use of OTR/INR instructions, bits 8 - 15 of a specified register being used.

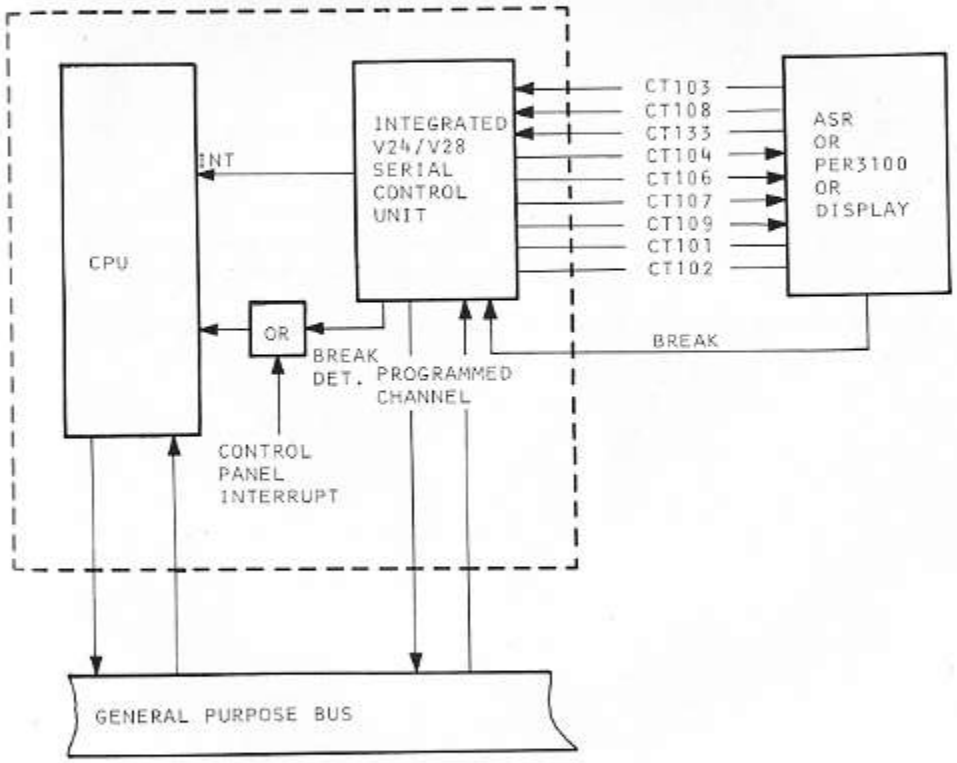

Figure 14.1 Integrated serial control unit