PHILIPS Data Systems

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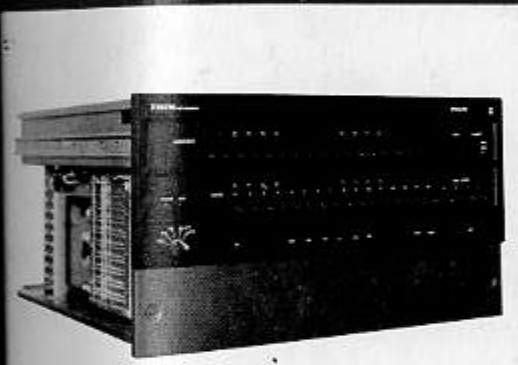
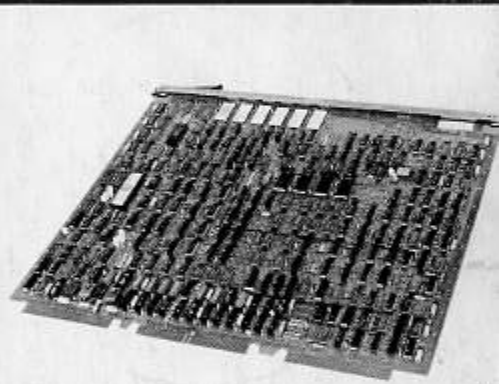
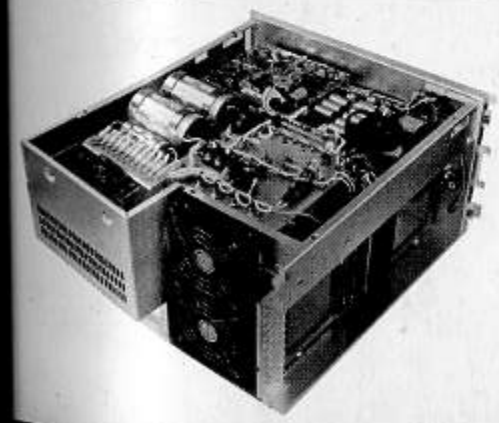
P856M/P857M System Handbook







Main features

- ASYNCHRONOUS GENERAL PURPOSE BUS
- SINGLE CARD MICROPROGRAMMED CPU
- INTEGRATED CONSOLE CONTROL UNIT
- CYCLE SPEED OF 1.2 OR 0.7 MICROSECONDS
- MEMORY MODULES OF 8 OR 16K WORDS
- MEMORY CYCLES INTERLEAVING
- MODULAR SYSTEM
- 16-BIT WORD ORIENTED
- 16 GENERAL PURPOSE REGISTERS
- MEMORY MANAGEMENT UNIT (P857M), 2K WORD PAGE SIZE
- FLOATING POINT PROCESSOR (P857M)
- PROGRAMMABLE REAL TIME CLOCK
- DIRECT, INDIRECT, INDEXED, INDEXED INDIRECT ADDRESSING
- 63 INTERRUPT LEVELS
- EXTERNAL REGISTER TRANSFERS
- HARDWARE MULTIPLY/DIVIDE, DOUBLE LENGTH ARITHMETIC
- AUTOMATIC STACK HANDLING
- REAL TIME CLOCK (20 MS, MAINS)
- INTEGRATED V24 SERIAL CONTROL UNIT
- POWER FAILURE DETECTION WITH AUTOMATIC RESTART
- MICRODIAGNOSTICS
- LOW AND HIGH SPEED DATA CHANNELS
- INTERFACES FOR INDUSTRIAL EQUIPMENT
- DATA COMMUNICATION
- POSSIBILITIES TO CONNECT ALL STANDARD PERIPHERALS
- SOFTWARE PACKAGE INCLUDES:
  STAND ALONE SOFTWARE
  BASIC AND BASIC REAL TIME MONITORS
  DISC AND DISC REAL TIME MONITORS
  MULTI APPLICATION MONITOR (P857M)
  SMALL REAL TIME MONITOR
  CASSETTE OPERATING MONITOR
  MONITOR EXTENSION FOR DATA COMMUNICATION
  ASSEMBLER, FORTRAN COMPILER, BASIC, FACT, LINKAGE EDITOR, OVERLAY LINKAGE EDITOR, CASSETTE EDITOR, UPDATE PACKAGE, LINE EDITOR, DEBUGGING PACKAGE, HARDWARE TEST PROGRAMS

P856M/P857M
System Handbook

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Preface

This handbook is one of a series of manuals which covers all aspects of the P856M and P857M mini computer system. It is intended to provide general information with respect to the system in the form of short descriptions of the component units and peripheral devices which comprise the system.

Because of the flexibility of the system it is possible to include non-standard and customer designed equipment within any system and where such possibilities exist the connection facilities available have also been generally described. A user should however refer to the more detailed publications within the series before using such facilities.

Great care has been taken to ensure that the information contained in this manual is accurate and complete. Should a user, however, find any errors or omissions, or wish to suggest improvements, he is invited to write his comments on the sheet provided at the end of this book and send it to:
Manual Writing Small Computers
at the address on the opposite page.

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Cabinet	- The basic structure containing 19'' racks
Rack	- The structure within the cabinet to which rack mounted units may be secured.
Basic Cabinet	- A cabinet in which the CPU is mounted.
Extension Cabinet	- A cabinet containing system equipment other than the CPU.
Mounting Box	- The rack in which the CPU is plugged.
Equipment Shelf	- The rack in which system equipment other than the CPU is plugged.
Standard Device Unit or Package	- One which is listed in the Catalogue.
Microdiagnostics	- A microprogram standard available on the CPU board, which tests panel drivers, data path, bus dialogue and memory.
Character	- One half-word: 8 bits.
MSI	- Medium Scale Integration.
LSI	- Large Scale Integration.
TTL	- Transistor to Transistor Logic.
ROM	- Read Only Memory.
PROM	- Programmable Read Only Memory.
MOS	- Metal Oxide Semi-conductor.
IPL	- Initial Program Loader.
GP BUS	- General Purpose Bus.
MMU	- Memory Management Unit.
FPP	- Floating Point Processor

The P856M and the P857M mini computers are general purpose digital processors designed for industrial and scientific applications.
These computers are the newest members of the successful P800M series family which were placed in all Western-European countries as well as in the United States and Japan.

The P856M and the P857M are fast, compact and easy to interface thanks to the asynchronous General Purpose Bus around which all I/O facilities are centered and two types of memory available. The P856M is the smaller computer of the two with a maximum of 32k memory. Memory modules for this computer are 8k 16-bit words with a cycle time of 1.2 μs. Also available are 16k 16-bit word memory modules with either 0.7 μs or 1.2 μs cycle time. If two 16k fast memory modules are used memory cycles interleaving is possible.

The P857M offers a tremendous increase in memory size and programming power thanks to a one-board Floating Point Processor and a one-board Memory Management Unit.
The Floating Point Processor gives a hardware execution of floating point instructions. The Memory Management Unit provides the user with two important features: it permits word and character addressing in up to 128k words memory *and* it implements memory protection on a 2k word page basis.
Together with a backing store, such as disc, the system offers a practically unlimited programming space and gives the user all the advantages of a real-time environment, under control of a Multi Application Monitor.
Standard memory modules are 16k 16-bit words with 0.7 μs cycle time. On option, 16k 1.2 μs cycle time memory modules may also be used.
The high speed memory allows interleaving when at least two 16k modules are used.

Standard features for both CPU's are:
- 16 hardware registers of which 14 are fully programmable
- integrated V24 serial control unit
- power failure/automatic restart
- line frequency real time clock (20 ms)
- general purpose bus
- 63 program interrupt levels
- direct access for up to 256 external registers
- direct memory access facility
- microprogrammed standard instruction set
- addressing for up to 32k 16-bit words
- hardware bootstrap loader

plus the following features particular to each CPU:

P856M
- microdiagnostics for automatic and step-by-step testing of the first 4k words of memory and CPU-CU dialogue.
- programmable Real Time Clock (option).

P857M
- microdiagnostics for automatic and step-by-step testing of the first 16k words of memory and CPU-CU dialogue.
- addressing extension for up to 128k words of memory through a Memory Management Unit MMU (option)
- memory protection on a 2k words page basis
- Floating Point Processor (option)
- programmable Real Time Clock (option).

All input/output transfers are handled via the General Purpose Bus. A comprehensive and powerful instruction set, including instructions such as multiply, divide, multiple store, multiple load, external register handling instruction and, for the P857M some extra instructions pertaining to the MMU facility, for table handling and extended memory addressing and the Floating Point Processor provide the programmer with a wide range of programming possibilities and fast execution of programs.

System software for the P856M comprises six monitors:
Basic Operating Monitor, Disc Operating Monitor, Cassette Operating Monitor, Basic Real Time Monitor, Disc Real Time Monitor, Small Real Time Monitor and a monitor extension to be used in a data communication application. The system software for the P857M is the same as for the P856M plus a Multi Application Monitor to be used in systems over 32k words.

Moreover the following processing and service software is available:

Assemblers, Linkage Editors, Overlay Linkage Editor (P857M only), FORTRAN, Real Time FORTRAN, Line Editor, Update Packages, Cassette Update, Debugging Package plus several utility packages.
BASIC (Beginners All purpose Symbolic Instruction Code) and FACT (Facility for Automation, Control and Test) conclude this wide range of software available to the user.

All system software for the P856M and P857M is compatible with the P852M system software except for the extended memory addressing software, which can only be usefully used on the P857M over 32k words.

A diagramatic representation of the system's components and input/output structure are shown by figures 1.1 and 1.2 respectively.

THE SYSTEM

The facilities offered to a user by the P856M and P857M minicomputer systems enable each user to produce a tailor made system to suit his own requirements, and thus avoid the need to purchase facilities which will never be used.

The ease with which a system may be constructed and enhanced, and the overall flexibility of the system are centered around the general purpose bus. This asynchronous bus is used for the interconnection of the system's main components: memory, peripheral device control units, transfer facilities, interrupt facilities and the central processing unit itself. Physically the bus may be of various lengths, to suit any particular configuration, and it consists of those lines required to make correct interconnection and operation between units possible.

Efficient operation of the system is organized by a full range of controlling software in conjunction with the interrupt system. The interrupt system is capable of handling up to 63 hardware levels and operates using the necessary bus lines concurrently and independently of data transfers or bus control operations.

Peripheral connection is also made easier by use of the bus and the availability of up to 64 input/output processor sub-channels for high speed data transfers provides the system with a powerful input/output capability. Organization of the channels is on a priority basis and any number of the channels may be in operation at the same time. Once in operation the input/output processors are able to control a transfer between a device control unit and memory using both the bus and a single break line connected directly between the control unit and the input/output processor controlling the exchange.

The central processing unit, connected within the system via the bus, is normally allocated bus time in accordance with the system requirements. However, the possibility exists for the central processing unit to be given the bus whenever this is necessary for system operation. Processor instructions are available to carry out all the normal arithmetic and logical processes necessary for the operation of the system, both at word and in certain cases character level. Input/output instructions exist for the control and operation of all standard peripheral device control units and, in addition, instructions exist to read and write to external

registers via the General Purpose Bus and, for P857M extended memory addressing, instructions to Move Tables and to load registers with addresses for Page handling. The Floating Point Processor permits the use of hardware for the execution of floating point instructions.

Memories
The memories consist of 1.2 μs or 0.7 μs cycle core memory modules connected via the General Purpose Bus. The 0.7 μs memories allow interleaving. It is possible to mix the 1.2 μs and 0.7 μs memories.

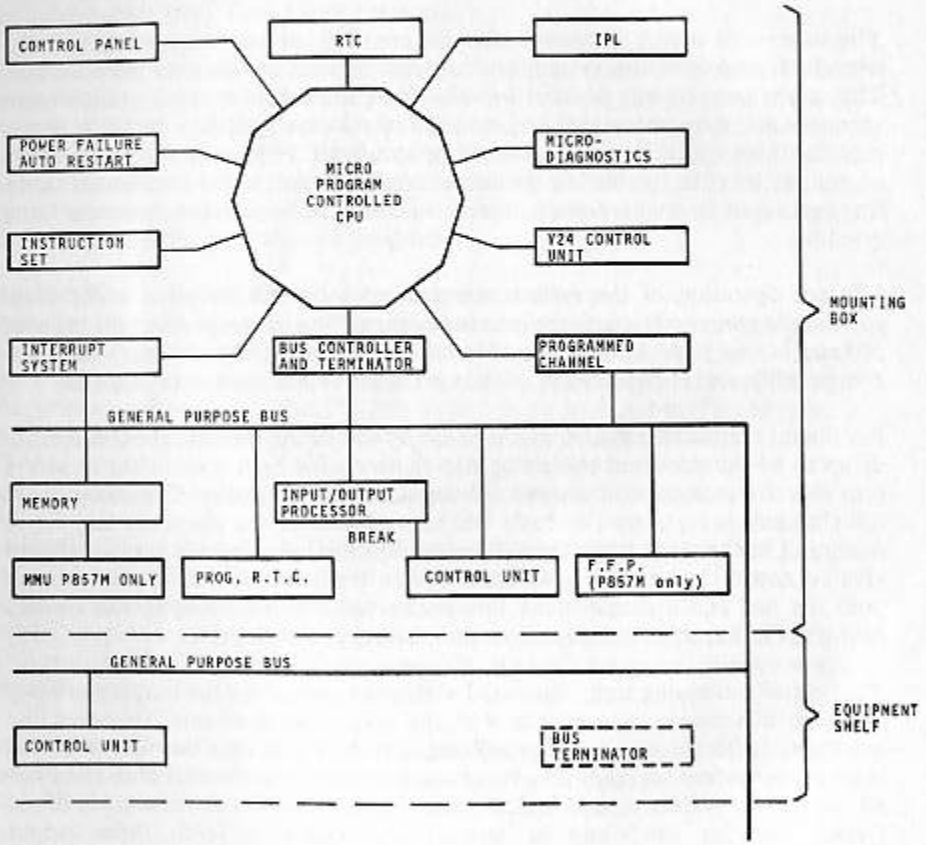


Figure 1.1 System Main Components

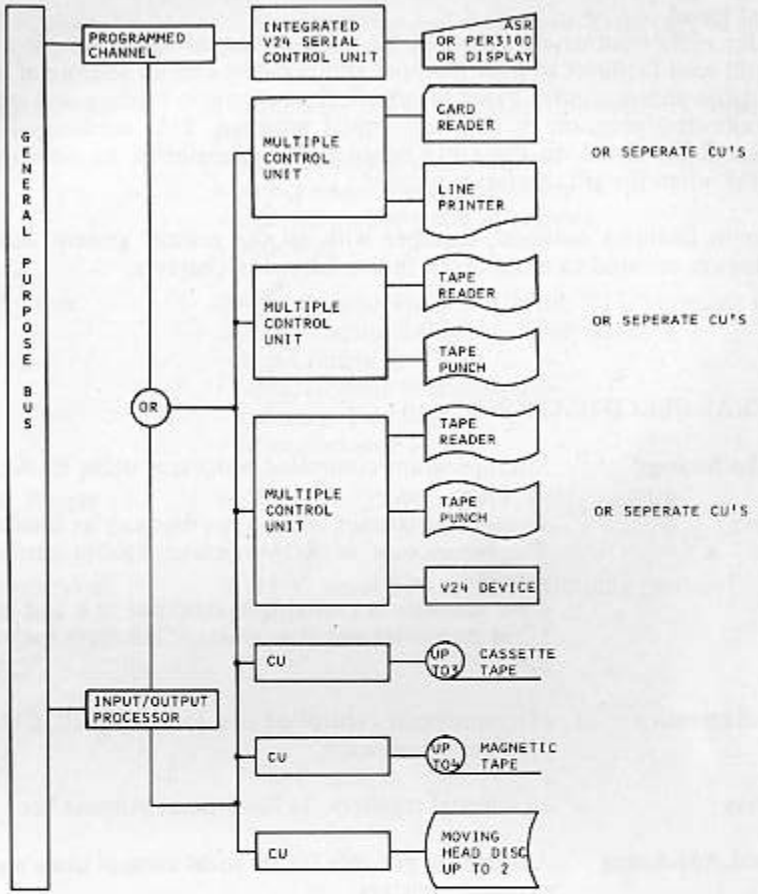


Figure 1.2 Survey of peripherals and their control units

Interleaving
Interleaving of the 0.7 μs read/write core memory permits a very fast execution of instructions. The access time comprises one read cycle after which the execution of the instruction starts immediately. To make full use of the interleaving capability the minimum memory size is 32k i.e. 2 modules of 16k where one module will contain the even addresses and the other module the odd addresses.

Control Panel
Operator press buttons are provided for normal manual operations, including load and read facilities to both memory and registers and an additional option is available at the control panel to enable the automatic loading and running of a bootstrap program to load any initial program. This bootstrap is held within a ROM fitted on the CPU board and is transferred to memory and executed when the IPL button is pressed.

The main facilities outlined, together with all the normal system and user facilities are covered in more detail in the following chapters.

GENERAL SPECIFICATIONS

CPU Technology
Microprogram controlled processor using ROM, TTL circuitry.

Memory
Coincident current ferrite core memory as standard.
The connection of ROM and/or PROM memory is possible.
Core memory is available in modules of 8 and 16k for 1.2 μs memories and in modules of 16k for 0.7 μs memories.

Microdiagnostics
Microprogram controlled test for data path, CU-CPU dialogue, memory.

Registers
16 internal registers, 14 for general purpose use.

External Addressing
Addressing possible for up to 64 control units and 256 external registers.

I/O Capability
Up to 64 control units may be connected within the system.
Two separate types of transfer channel:
1. Programmed Channel capable of transfer rates up to 30k words/sec. depending on the method of programming used.
2. Up to 8 Input/Output Processor Channels, each controlling up to 8 separate devices on a priority basis and capable of transfer rates up 833k words/sec for memories of 1.2 μs and 1.2Mw with the fast memory. Each device control unit uses a separate break line connected directly between itself and the appropriate input/output processor.

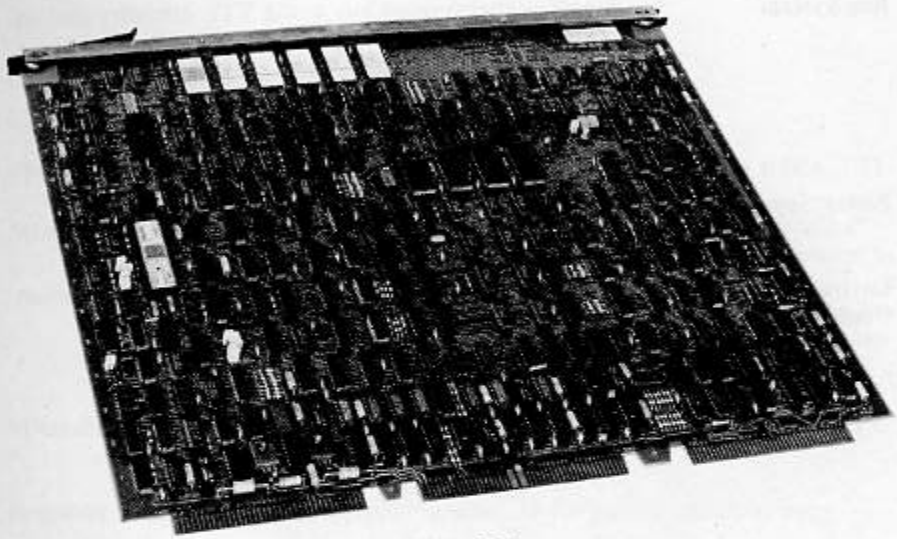
Word Format
16-bit instruction and data word. Data may be handled as two separate 8-bit characters.

Instruction Set
Instructions using 8 different methods of forming an operand, including:
- short and long constants
- direct and indirect addressing
- address and operand in register
- indexing

Bus System
Single asynchronous bus using TTL circuitry and incorporating the following subsections:
- Bus Control
- Data/Command Exchanges
- Interrupt Handling
- Miscellaneous

Power Supply
100V, 115V, 220V or 240V, 50Hz or 60Hz
Standard: 220V 50Hz

Environmental Conditions
0°-45°C, up to 90% relative humidity (without condensation)



P856M CPU

Figure 2.1 shows the main units of the system's hardware structure in block form. Explanations of the memory, GP Bus, interrupt system and input/output facilities are covered in detail in later chapters.

CENTRAL PROCESSING UNIT

The main components of the CPU are:

Arithmetic Unit (ALU)
The circuits which make up this unit enable the addition, subtraction or logical combination of the two 16-bit inputs to be available as a single 16-bit output. In addition the state of the output with reference to a positive, negative, null, or overflow condition is available, and an indication is also given when the ALU output is less than decimal 128 if this output is to be used as a memory address for stack operations. Overall control of the unit is exercised by the micro program held within the system's control ROM.

P Register
This register is used to hold the address of the next instruction to be carried out. It is incremented in steps of two if the program is to carry on in sequence or altered to hold the required new address if a branch is to be carried out. This register is physically only 15 bits, corresponding to bits 0 to 14 of a full 16-bit address word.

The PSW Register
This register is divided into three parts which together form one 16-bit word known as the Program Status Word. Certain instructions and hardware functions cause this word to be stored in a memory stack whenever it is required to be saved. Program action is required to restore the saved word and whilst it is held in the memory stack program action may be carried out to alter the contents of the word.

The PL Register
Six bits used to hold the priority level of the program that is running. Control of this register is exercised by the interrupt system.

The CR Register
Two bits used to hold the state of the result of, or the response to, certain instructions. Control of this register is exercised by the microprogram held within the system's control ROM.

The GF Register
Up to eight bits which are used to record the general status of the system.

The Scratchpad
The scratchpad consists of four 15 × 4-bit read/write memory circuits arranged to give fifteen 16-bit registers A1 to A14, A15. These registers may be addressed from either the instruction being carried out or from switches on the operator's control panel. Overall control of the scratchpad is exercised by the microprogram held within the system control ROM. The specific designation of registers within the scratchpad is:

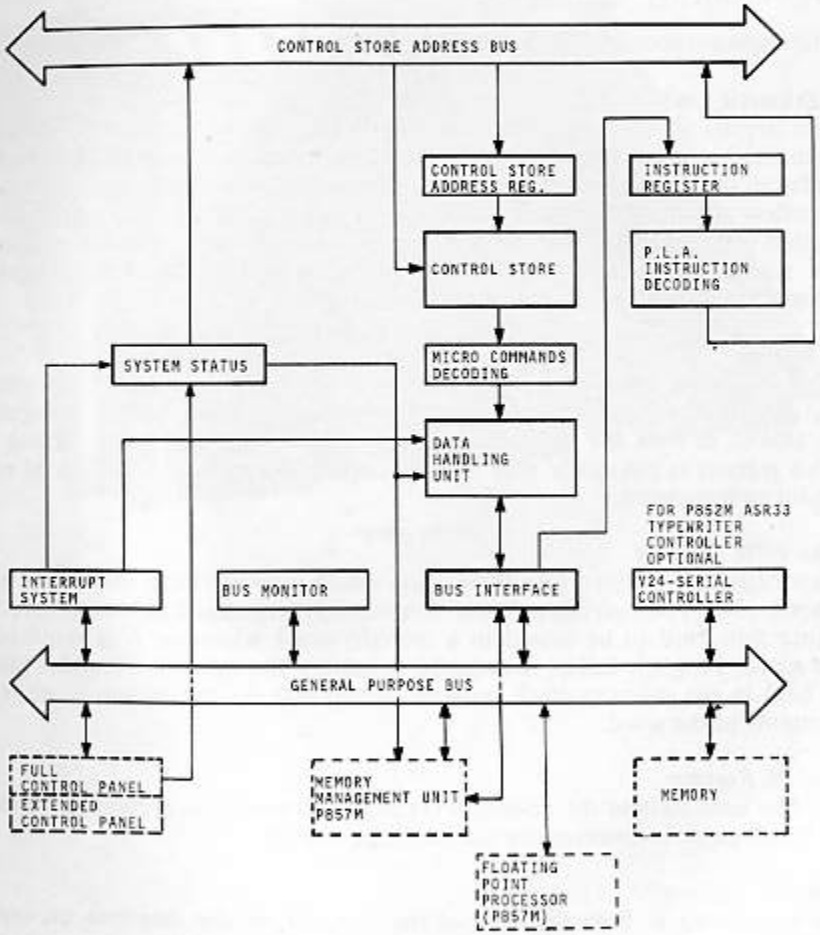


Figure 2.1 General structure of CPU

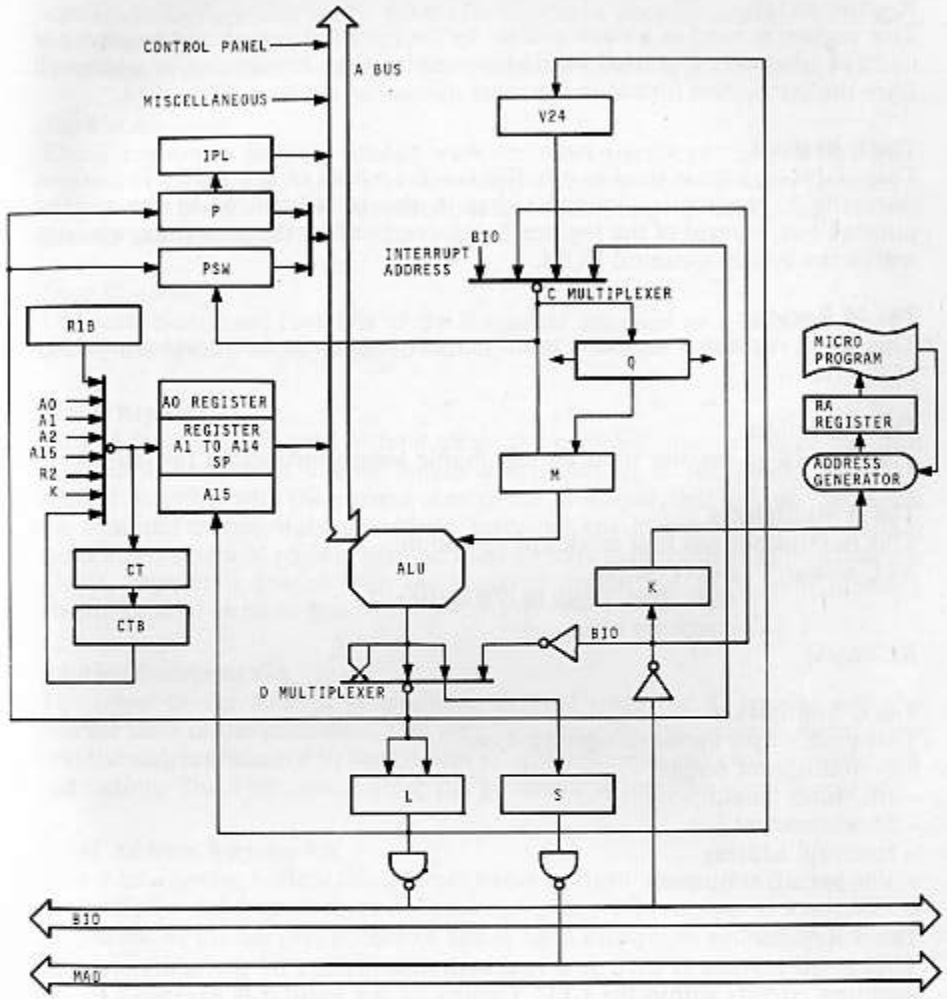


Figure 2.2 Data flow in Data Handling Unit

Registers A1 to A14
These registers are addressed from the instruction format whilst the processor is operating and may be used to hold one or both of the operands of an instruction, and possibly the result. They may also be used as addressing and indexing registers with respect to memory.

Register A15
This register is used as a stack pointer by the interrupt system and as such it is updated whenever it is used for memory addressing. It may also be addressed from the instruction format in the same manner as registers A1 to A14.

The L Register
This 16-bit register is used as a buffer for the output of the ALU. The output from the L register is directed either to the scratchpad or to the general purpose bus, control of the register being exercised by the microprogram held within the system's control ROM.

The M Register
This 16-bit register is used as a multi-purpose register in the input/output-loop of the ALU.

The Q Register
This is a 16-bit register used during double length instruction operations.

The D Multiplexer
This multiplexer has four modes of operation:
ALU output direct output
shift right. Input to S Register
character swap
BUS input

The C Multiplexer
This multiplexer performs operation on:
- D multiplexer output
- BIO lines output
- Short constant
- Interrupt address
- V24 serializer output

The S Register
This 16-bit register is used as a multi-purpose register by the addressing and counting circuits within the CPU. Control of the register is exercised by the microprogram held within the system's control ROM. The three uses of the S register are:

Normal Addressing
Input to the S register is from the fifteen most significant bits of the output of the ALU. The output of the S register is used for memory, external register, or device addressing, via the general purpose bus. The S register must be reloaded for each change of address.
For the P857M CPU, when running in user mode, only the 12 least significant bits of the S register are sent to the General Purpose Bus, whilst the 4 most

significant bits are sent to the MMU for logical to physical address translation (see page 5-1).
In system mode the 16 bits of the S register are used in the normal way.

Stack Addressing
The S register is initially loaded with the most significant fifteen bits from register A15, via the ALU. It is then used as a downward counter to address consecutive words in the memory stack. Addressing is carried out via the general purpose bus.

Loop Counter
The least significant four bits of the S register are used as a loop counter for use by the system microprogram.

The K Register
This 16-bit register is used to hold either the complete instruction or the most significant word of a double length instruction. It is the contents of this register, together with the current state of the processor, that are used to access the required microprogram words to carry out any instruction and in certain cases bits from the K register are also used directly in the control of instructions. The K register is loaded with the required instruction word from memory via the general purpose bus.

Address Generator GA
The input to the address generator is derived from the K register and the current state of the processor. The unit then encodes the relevant information into the address required by the control microprogram to carry out the particular instruction. The 9-bit output from the generator is input to the RA register.

ROM Address Register RA
This 9-bit register buffers the address being used to access the current micro instruction word from the control microprogram. The register is loaded from the output of the address generator and is used directly to address the control ROM.

Control ROM and Microprogram
This section is composed of six ROM ICs. Each IC contains 512 eight-bit words which are accessed by nine addressing inputs. Addressing from the RA register is applied in parallel to the six ICs to obtain 512, fourty-eight bit words of memory.
The microprogram is held in the ROM and exercises direct control over the data paths and timing of the CPU.

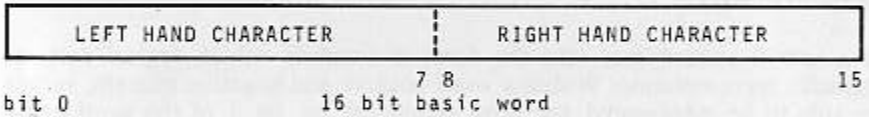
Control and Data Flow
The control and data flow of basic instructions is shown in Chapter 8.

Single Precision

The basic word used within the system is 16 bits, and as such it may be represented by four hexadecimal symbols in the range 0000 to FFFF. Bits within the word are numbered from 0 to 15, bit 0 being the most significant bit. Data may be represented as single precision signed integer contained in one word as follows:

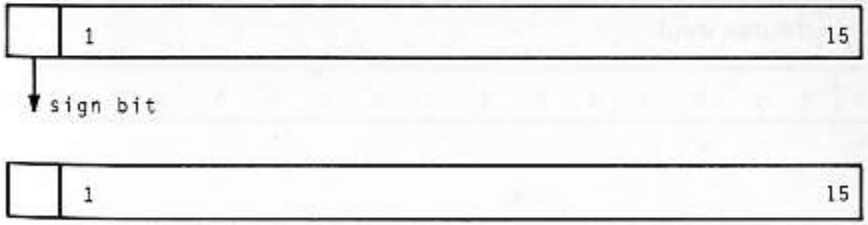
where bit 0 is used as the sign bit, set to zero for positive data and to 1 for negative data.

For programming purposes the word may be divided into two 8-bit characters which may be used independantly by certain processor actions, bits 0 to 7 of the word representing the left hand character and bits 8 to 15 representing the right hand character.



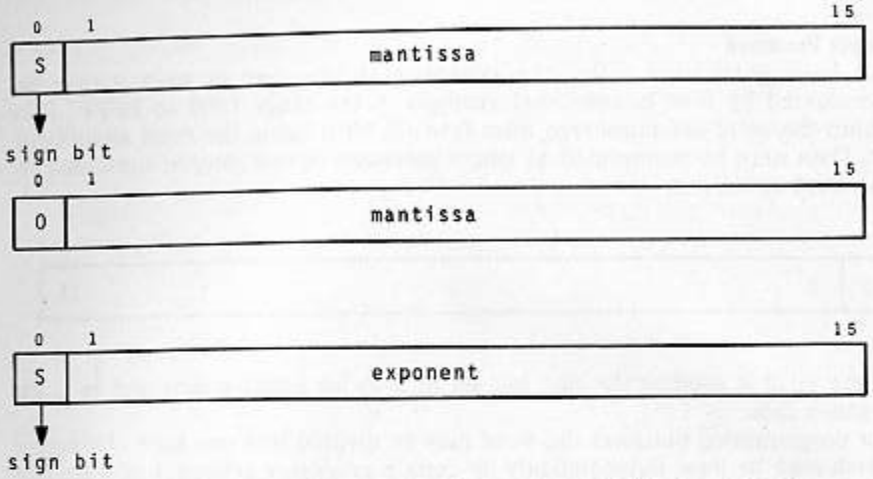
Double Precision

In double length instructions data may also be represented as a double precision signed integer, contained in two words as follows:



The sign bit of the least significant word is not used and is usually set to 0. This means that 30 bits are available for data representation.

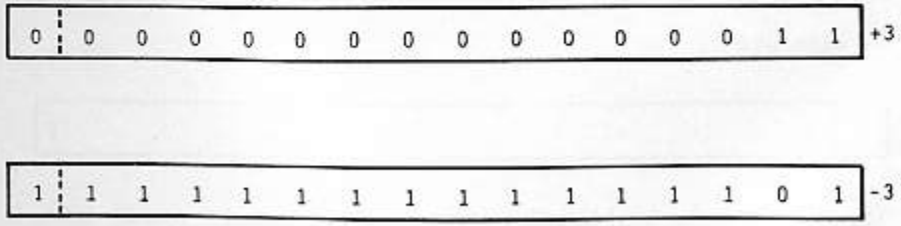
Floating Point Data
Real numbers are place in three successive words. The first two contain the mantissa and the third the exponent.



For a more detailed description see also chapter 6 on the Floating Point Processor.

DATA FORMAT

Data within a word may take the form of numeric values, logical data, or character representation. Within a word positive and negative numeric values are able to be represented, the most significant bit, bit 0, of the word being used to indicate the sign of any value. Positive values are represented by making the sign bit equal to 0 and using the remaining fifteen bits to express the numeric value in binary. Negative values are represented by making the sign bit equal to 1 and expressing the required numeric value by its 2's complement in the remaining fifteen bits.
The figure below shows the representation of the numeric values +3 and −3 within the data word.



Representation of Numeric Values

Numeric values represented and used within characters may only specify positive values to a maximum of 8 binary bits, no sign bit being used by either character.

Logical data may be held and used in either whole word or character format and no sign bit is used, data being bit significant within the complete word or character.

Data representing standard alphanumeric and control characters may be held within the separate characters of the data word and will be treated as either numeric values or logical data depending on the instructions carried out when using such data.

Core memory is available in modules of 8k or 16k 16-bit words with a cycle time of 1.2 μs or 0.7 μs up to maximum of 32k for the P856M and 128k for the P857M. Each module consists of a single printed circuit board which is mounted within the mounting box. Connection to the system is by pluggable connectors to the General Purpose Bus and provision is made for the protection from loss or detorioration of data during power on/off sequences and in the event of any power failure.

All memory modules offered are able to operate in either word or character mode and special character handling instructions are available to provide a useful and efficient facility with respect to character buffering and transfers. Character mode operation enables the contents of the least significant eight input/output lines to be either set from, or written into either the left hand or right hand character of the addressed memory location. In all such operations the unused character is left unaltered.

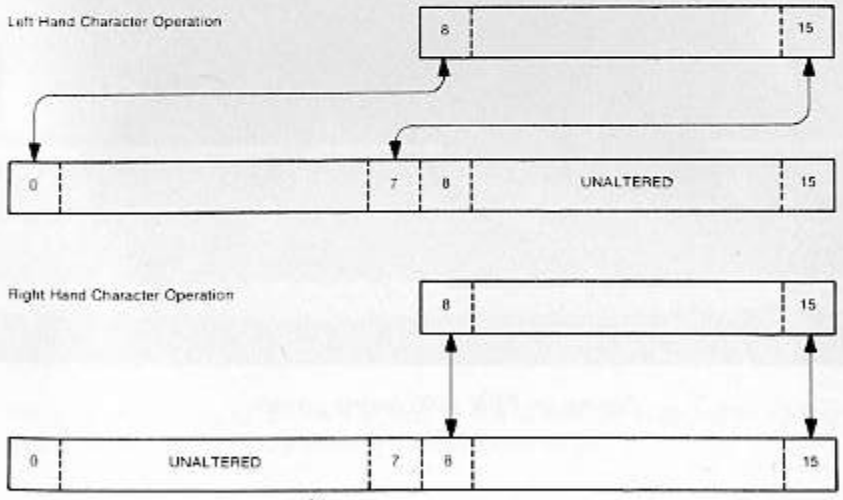
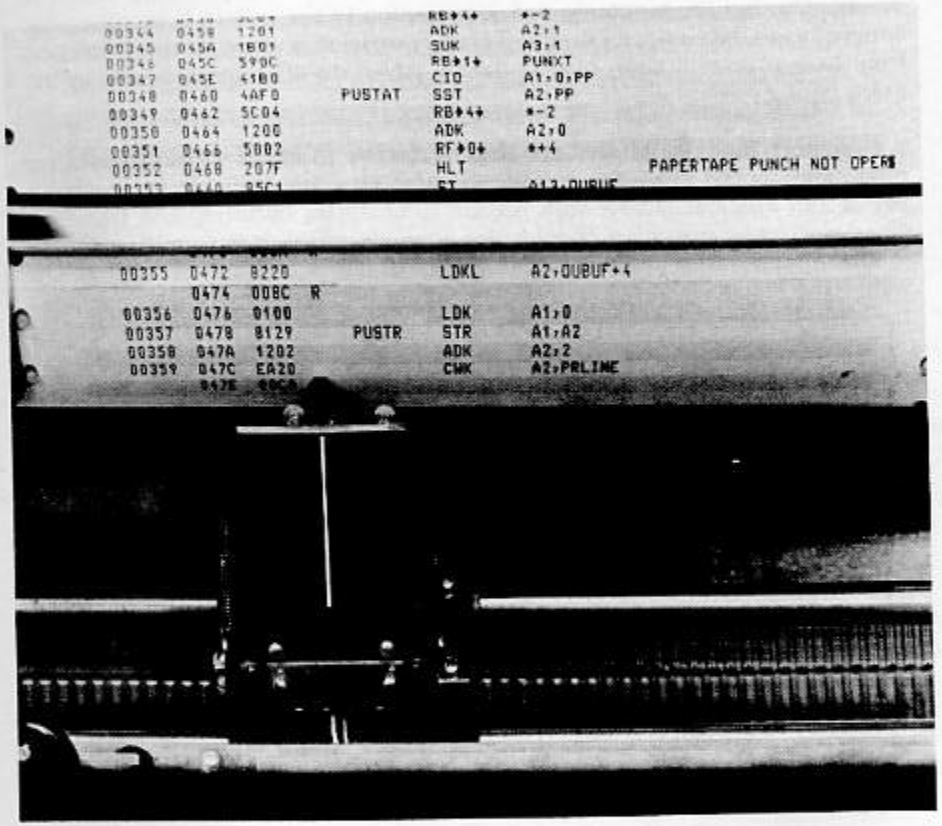


Figure 4.1 Operation of memory in character mode



Listing on PER 3100 matrix printer.

MEMORY ADDRESSING

Depending upon the type of instruction or operation being carried out the memory may be addressed in words or characters for programming purposes. Bits 0 to 14 of the address are used to access memory in word mode, bit 15 being unused and insignificant. When operating in character mode all sixteen address bits are used, bits 0 to 14 addressing the word location required and bit 15 addressing the character. With bit 15 set to 0 the left hand character is addressed, bit 15 set to 1 addresses the right hand character.

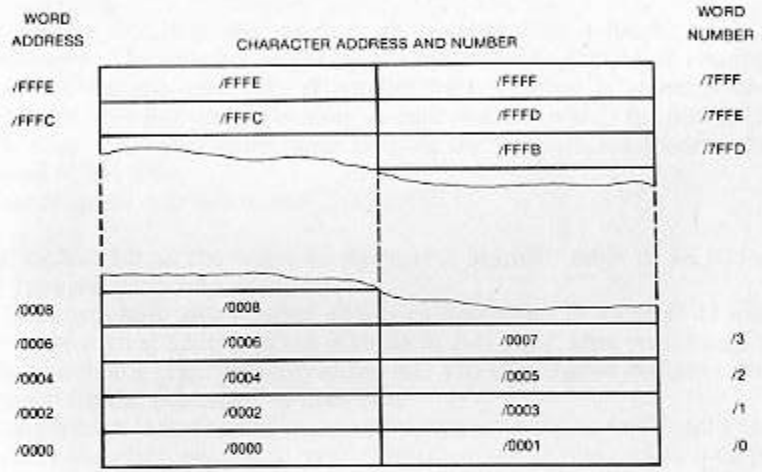


Figure 4.2 Layout of words and characters in memory.

Word addresses written with the least significant bit present will be addressed ignoring this bit.

Memory addressing in an environment >32k is entirely transparent to the user and is taken care of by the Memory Management Unit.

DESCRIPTION

The Memory Management Unit is a feature of the P857M computer which uses Virtual Addressing and allows to extend memory addressing over 32k op to 128k words. It permits dynamic program relocation in multitask programming under control of the Multi Application Monitor and offers a memory protection facility.
The MMU cannot by used with the P856M.
Special instructions are required by the MMU to handle the memory addressing.

The system considers the memory as consisting of n blocks of 2k words, called pages. The monitor is always loaded at the beginning of memory from the lowest address upwards. When the user program is called it is loaded behind the monitor and it is split in pages of 2k, which do not need to be contiguous. Moreover, only those parts of the program are loaded which are required at the time.
A user program may not exceed 32k words.

In order to address the pages in memory a segment table of 16 × 16 bits is built for each program called.
The user program uses relative addresses contained in 16 bits. At execution time these logical addresses are divided in two parts. One part, bits 0 to 3 included, contain a segment address and bits 4 to 15 included contain the relative address from the beginning of the page.
The segment address refers to an entry in the segment table and the MMU translates the entry, pointed to by the 4-bit segment address, into a 6-bit physical page number which, together with the 12-bit displacement value, produces an 18-bit address.

If the running program has less than 16 pages loaded in memory the unused words of the segment table have a protection bit set.

In system mode, see page 13-10, the MMU does not translate the 4-bit segment addresses as the system software routines use absolute addresses.
To transfer in this mode data from a system to a user area special instructions which have a source table address, destination address and length as parameters, permit to communicate between the user and system areas.

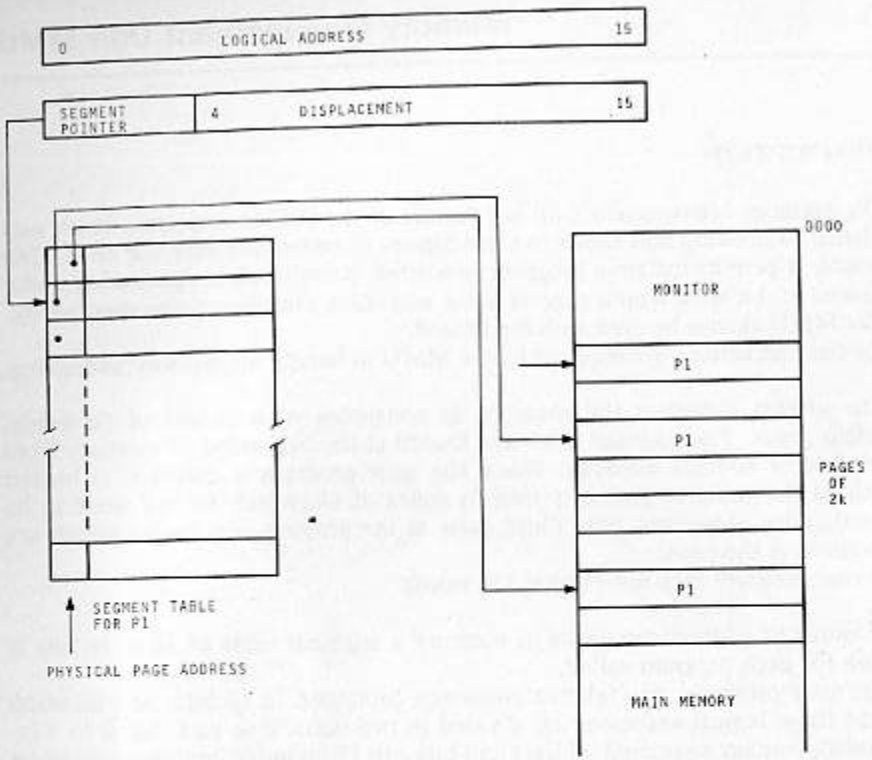


Figure 5.1 MMU Operation.

Layout of segment table word
The MMU and the operating system control the contents of the segment table words. The bits in this word have the following meaning:

bits 0–5 Physical Page address.

bit 6 Page Error indication. This bit is set by the Operating System for those pages which do not belong to the addressing environment of the running program. By checking this bit the MMU activates a 'Page Fault' signal when a wrong or missing page is tried to be accessed.
This bit is not used for system programs.

bit 7 Read Only page. This bit is set when the relevant page is protected against overwriting. This feature allows to share the page among several user programs.

bit 8 Modified Page. This bit is set by the MMU when a write operation took place in this page. If so, the page need to be swapped out again to the backing store before a new page is loaded. If the bit remains zero the page may be overwritten which saves time.

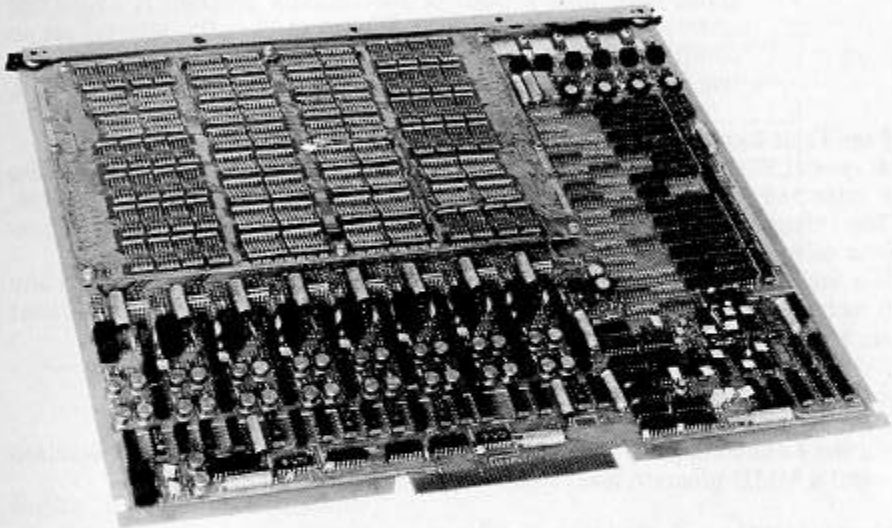
bit 9 Overflow. The setting of this bit depends on the value in bits 10-15 included.

bits 10-15 Counter. A 6-bit counter is associated with each page descriptor. All counters are incremented at regular time intervals. This interval, which depends on the memory speed, is chosen at system generation time in a ratio 1 to 256. During execution of a program, each time a page of the running program is called the counter is reset to zero. If a counter reaches the interval set an overflow bit is set. When space in memory is required the Operating System swaps out those pages which have the overflow bit set.

Page Fault handling
A special interrupt *Page Fault* is given when an attempt is made to write into a protected page or when a missing or wrong page is tried to be accessed. The interrupt line is wired from the MMU to the CPU and it has a priority over other internal or external interrupts.
If a fault is detected the execution of the running instruction is stopped and if necessary, exchange parameters are updated to resume the execution later on. Moreover three words are stored in the system stack:

- the address of the instruction which caused the page fault interrupt
- the PSW
- a word containing the page address of the page in which a fault was detected and a MMU program level coded on the MMU board.

Next the CPU is switched to the Inhibit state and the computer to system mode. The MMU program level is loaded in the PLR register and a branch is made to an interrupt routine address.
The interrupt routine does not require an RIT instruction to reset the interrupt as the Page Fault interrupt is automatically deactivated.



16k Memory Module 1.2 µs

Introduction

The Floating Point Processor is an optional, high speed arithmetic processor which may be included in the P857M system.
It performs by hardware, single precision, all floating point arithmetic operations.
The processor is contained on one board and must be plugged in the *third* slot of the M4 or M5 mounting box, also when no Memory Management Unit is used. The power consumption is + 5 V, 6.0 Amps.
Figure 6.1 shows the connection of the FPP in the system.

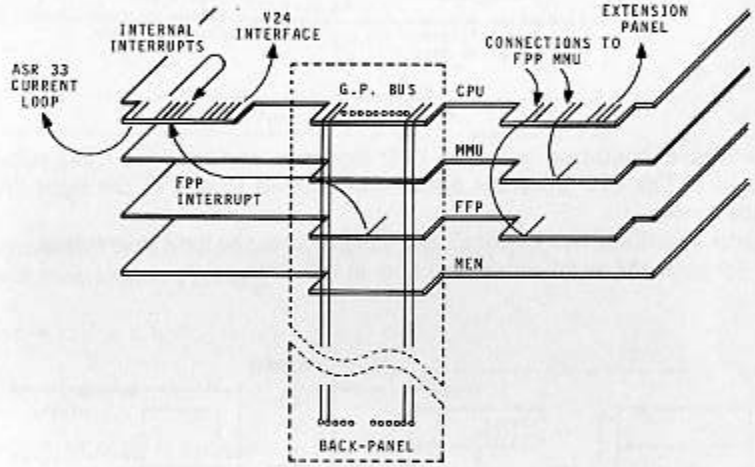


Figure 6.1 Connection of Floating Point Processor

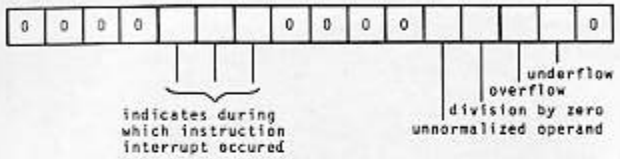
Operation

The board contains three 16-bit accumulators FPA holding the result of a floating point operation or the floating point operand or the first floating point operand where the second floating point operand is temporarily placed in three other 16-bit registers.

Program instructions are fetched and decoded by the CPU. The significant bits of each instruction, i.e. op.code, mode, bits etc. are also copied in an instruction register on the FPP board.
When a floating point instruction is encountered in the program the Floating Point Processor is activated by the CPU and the latter stops.
Some decoding of the instruction register contents takes place on the FPP board

and an arithmetic unit on this board is signalled the type of operation it has to perform.
The arithmetic unit takes the information to be operated upon from the contents of the FPA, registers A1 and A2, the contents of consecutive memory locations.

The result is stored in FPA, or A1 and A2, or a number of consecutive memory locations.
During or immediately after the execution a status register is reset to either zero (no errors) or bits in this register are set to 1. The contents of the status register may be:



Any abnormal condition gives an FPP interrupt and sets the CPU condition register to 3. The FPP interrupt must be connected to one of the eight internal interrupt levels.
If no error condition was obtained the CPU fetches the next instruction.
Figure 6.2 gives the architecture and flow in the FPP.

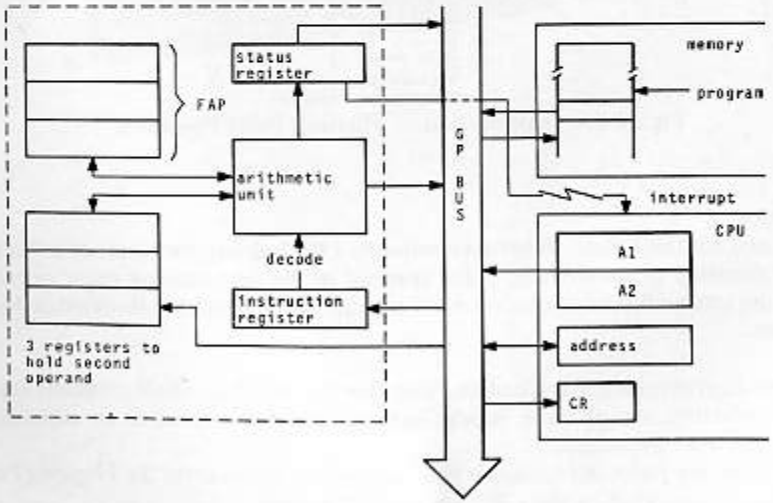
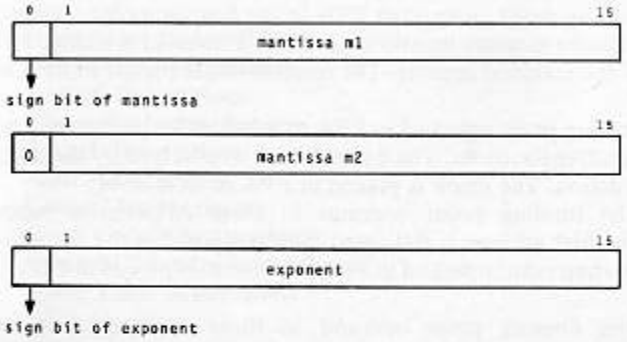


Figure 6.2 Floating Point Processor

Floating Point Format
The Floating Point Processor handles data of the following format:

Floating Point Data
Floating Point Data are real numbers contained in three consecutive 16-bit words. The first two words contain the mantissa which is a left normalized, double precision number.
The exponent is held in the third word as a single precision integer.



The sign bit of the second mantissa word is always zero.
The mantissa scale is between:

positive: $+\frac{1}{2} < m < 1^{-E}$

where $\varepsilon = 2^{-30}$

negative: $^{-}1 < m < -\frac{1}{2}^{-E}$

The exponent scale is between: $-2^{15} < E < +2^{15}-1$

A floating point number is: $(m1,m2) \times 2^{E}$, where E = the exponent.
The absolute value is: | DATA | $< 10^{9868}$. The accuracy is in 9 decimal digits.

The Floating Point Processor also allows the conversion of floating point data to integer format and vice versa.
In that case the Processor permits operations with single precision integers (on 16 bits) and double precision integers (on 32 bits, the most significant bit of the second word being 0).

Floating Point Instructions

Floating Point Instructions use the same type of addressing modes as the remainder of the P857M instruction set.

A survey of the Floating Point Instruction Set is:

FFL Convert the double precision integer to a floating point operand. Store the result in FPA.

FFX Convert a floating operand in FPA to a double precision integer. The result is placed in A1 and A2.

FADR Add the floating point operand in FPA to the floating point operand in three consecutive memory locations. The first address is indicated by the contents of the specified register. The result is either placed in FPA or in memory.

FAD Add the floating point operand in FPA to the floating point operand in three consecutive locations. The first address is indicated by the address in the instruction. The result is placed in FPA or in memory.

FSUR Subtract the floating point operand in three consecutive memory locatons, the first address is indicated by the register in the instruction, from the floating point operand in FPA. The result is placed in FPA or in memory.

FSU Subtract the floating point operand in three consecutive memory locations, the first address is given by the address in the instruction, from the floating point operand in FPA. The result is placed in FPA or in memory.

FMUR Multiply the floating point operand in FPA by the floating point operand in three consecutive memory locations, whose first address is given by the register in the instruction. The result is stored in FPA or in memory.

FMU Multiply the floating point operand in FPA by the floating operand in three consecutive memory locations, whose first address is pointed to by the address in the instruction. The result is stored in FPA or in memory.

FDVR Divide the floating point operand in FPA by the floating point operand in three consecutive memory locations, whose first address is given in the register specified in the instruction. The result is placed in FPA or in memory.

FDV Divide the floating point operand in FPA by the floating point operand in three consecutive memory locations, whose first address is pointed to by the address in the instruction. The result is placed in memory or in FPA.

FLDR The contents of three consecutive memory locations are placed in FPA. The first memory location is indicated by the register in the instruction.

FLD The contents of three consecutive memory locations are placed in FPA. The first memory location is pointed to by the address in the instruction.

FSTR The contents of FPA are stored in three consecutive memory locations. The first address is indicated in the register in the instruction.

FST The contents of FPA are stored in three consecutive memory locations. The first location is pointed to by the address in the instruction.

See Chapter 7 for instruction execution times.