Four types of control panel may be used for mounting:

- Full Control Panel
- Extended Control Panel
- Mini Panel
- Portable Panel.

FULL CONTROL PANEL

The Full Control Panel is the standard control panel for the P856M. It is 2U (88.90 mm) high.

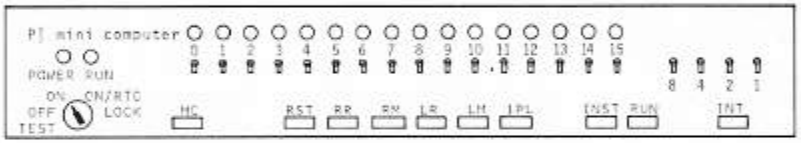


Figure 12.1 Full Control Panel

The facilities available on the full control panel are:

Safety Key Switch
A five position key operated switch providing the main on/off facility. The five positions are:

1. TEST - *Micro diagnostics*
In this position an elementary system test can be performed without any external tool. For a description of the microdiagnostics see page 14-7.

2. OFF - *Power off*

3. ON - *Power on*
In this position an elementary system test can be performed without any external tool. For a description of the microdiagnostics see page 14-7.

4. ON/RTC - *Power on/RTC on*
In this position the CPU is able to run with the Real Time Clock on. All the remaining control panel switches are effective.

5. LOCK – *Power on/RTC on*
In this position the CPU is in run mode with the Real Time Clock on. All the remaining control panel switches with the exception of the INT button are inhibited.

Display Lamps

1. Power Lamp
Situated above the Safety Key Switch, lit when the Safety Key Switch is in all but the Off position and power is being supplied to the system.

2. Run Lamp
Situated above the Safety Key Switch, lit when the CPU is operating in Run mode.

3. Data Lamps
Sixteen lamps situated one above each data switch and numbered 0 - 15. The lamps are lit to indicate the contents of the registers, memory, or status word depending on the settings of other control switches. A 1 bit is indicated where a lamp is lit.

Data Switches
Sixteen numbered data switches. Each switch is a two position switch used for loading the appropriate data bit into a register or memory, depending on the setting of other control switches. A 1 bit is loaded when a switch is in the up position.

Register Address Switches
Four switches mounted to the right of the data switches and used to code the address of the register to be used when reading or loading a register from the Data Switches. The switches are numbered with the address value they represent in binary (8, 4, 2, 1), giving an addressing capability of 0 - 15.

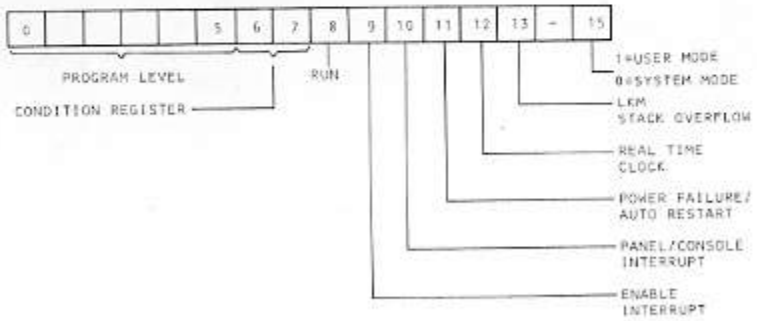


Figure 12.2 Display of status

Control Buttons
The five control buttons are situated nearly centrally beneath the Data Switches. Each button is spring loaded to return to its original position after being depressed and selects and initiates a specific function:

1. RST – *Read Status*
   Depressing this button causes the contents of Program Status Word register (Pl.CR.GF.) to be displayed on the lamps.

2. RR – *Read Register*
   Depressing this button causes the contents of the register addressed by the Register Address Switches to be displayed on the Data Lamps.

3. RM – *Read Memory*
   Depressing this button causes the contents of the memory location addressed from the contents of the P Register to be displayed on the Data Lamps. The contents of the P Register are also incremented by 2.

4. LR – *Load Register*
   Depressing this button causes the value set on the sixteen Data Switches to be loaded into the register addressed by the Register Address Switches. The value is also displayed on the Data Lamps.

5. LM – *Load Memory*
   Depressing this button causes the value set on the sixteen Data Switches to be loaded into the memory location addressed from the contents of the P Register. The value is also displayed on the Data Lamps and the contents of the P Register are incremented by 2.

Mode Buttons
The two mode buttons are situated beneath Data Switches 14 and 15. They select and initiate the following modes of operation.

1. INST – *Single Instruction Mode*
   Depressing this button causes the CPU to execute the instruction addressed from the contents of the P Register, and then stop.

2. RUN – *Run Mode*
   Depressing this button causes the CPU to execute the instructions of a program as directed by the program and commencing at the instruction addressed from the contents of the P Register.

Service Buttons
There are three service buttons:

1. MC – *Master Clear*
   Situated beneath Data Switch 0
   Depressing this button raises the master clear level throughout the system whilst it is depressed, causing a general reset of all the associated logic.

2. INT – *Interrupt*
   Situated beneath the Register Address Switches.
   Depressing this button raises a control panel interrupt.
   This button is the only control operative when the Safety Key Switch is in the LOCK position.

3. IPL – *Initial Program Loader*
   Situated beneath Data Switch 10.
   This button will only be present if the IPL option is fitted. In such cases, when the button is depressed it causes the Initial Program Loader to be loaded into central memory and the cpu to be started. Loading is carried out from the device and via the channel specified by the setting of the sixteen Data Switches.

TRANSPORTABLE PANEL

This panel is a free standing full control panel. It is fitted with a connector to enable it to be connected in place of a fixed full control panel or minipanel for mainly servicing purposes.

MINIPANEL

The minipanel may be fitted, on option, to replace the full panel and offers the following facilities:

1. Safety Key Switch
2. Interrupt and Start Buttons
3. Power and Run Indicators.

EXTENDED CONTROL PANEL

The Extended Control Panel is a 4U (177.80 mm) high panel which may be mounted when the CPU is plugged into the 10-slot M4 or M4M box or the 17-slot M5M mounting box (standard for P857M).
This panel permits to have an address and its contents displayed at the same time. Moreover the panel allows debugging facilities as processing may be stopped at any address set previously on the upper row of switches. The user may then load new data.
Addressing from this panel is word oriented.

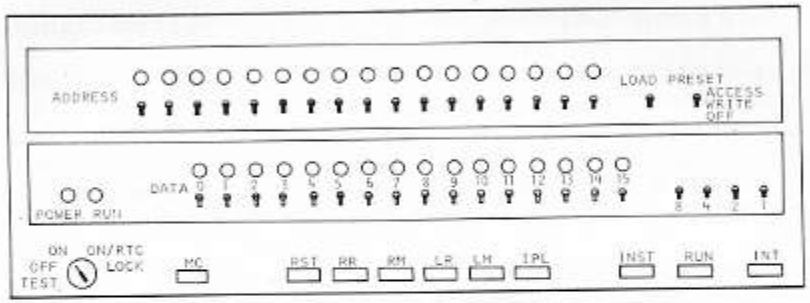


Figure 12.3 Extended Control Panel

The functions of the switches and displays are:

Display lamps
Seventeen lamps situated one above seventeen address switches. When the computer is running the lamps are lit to indicate addresses on the upper part of the panel and data on the display lamps of the lower part. When the CPU stops the contents of the next instruction's address is displayed on the lower part and the address of the instruction on the upper part.

Address switches
Seventeen address switches on the upper part of the panel. Each switch is a two position switch used for loading the appropriate address pattern. A 1 bit is loaded when a switch is in the 'up' position.

LOAD spring-loaded switch
Used to load an address in an address register contained in the control panel. The required address is set on the address switches. The LOAD switch is pressed downwards and the address is displayed on the address lamps.

PRESET switch
A three position switch for debugging purposes:

ACCESS - *stop on memory access*
In this position the CPU stops when a physical address generated by the CPU is identical to the pattern coded on the address keys. If the address is detected the relating instruction is executed and the CPU goes in the idle state.

WRITE - *stop when writing into memory*
In this position the CPU only stops if a store operation is performed in the location whose address was set previously on the address keys.

OFF
The switch is set in this position when debugging is not required.

Reading and loading memory is realised by using the RM and LM buttons. The instruction counter P remains unaffected during these operations as only the address register in the control panel is incremented. It is therefore not necessary to reload P before restarting the program.
The use of the RM and LM buttons is slightly different when the Extended Control Panel is used compared to the description under Full Control Panel.

Read Memory Procedure
- First load the address register with the required address (see LOAD addr).
- Press RM button. The contents of the memory location is displayed on the data lamps.
- The control panel register is incremented by two and the next address is displayed on the address lamps.
  Each time the RM button is pressed the address register is incremented and the contents of the next memory location appears on the data lamps.

Load Memory Procedure
- First load the address register with the address required (see LOAD addr).
- Set the value to be loaded on the data switches.
- Press LM button.
  The value is displayed on the data lamps. The address register is incremented and displayed on the address lamps.

All other pushbuttons and switches have the same meaning as described under FULL CONTROL PANEL.

The basic loading and operating facilities are all carried out at the CPU control panel by the use of the control panel switches. Facilities exist at the panel to enable an operator to load and display selected memory locations and registers, to start the CPU, and to raise a control panel interrupt. In addition an optional facility is available to enable the direct loading of an Initial Program Loader, or similarly written program, from various devices.

PROGRAM LOADING

Program loading may be carried out in 4 separate stages:

1. LOAD BOOTSTRAP - (MACHINE CODE)
2. LOAD INITIAL PROGRAM LOADER - (MACHINE CODE)
3. LOAD SYSTEM OR USER PROGRAM - (OBJECT CODE)
4. LOAD USER PROGRAM - (OBJECT CODE)

Bootstrap
This program is a basic program used to load more sophisticated loader programs. The bootstrap will only load programs which are written in machine code (binary form) and will normally only carry out a checksum to determine errors.

Initial Program Loader
The programs which are classed as initial program loaders are able to load object code clusters into memory and may contain error reporting and other facilities required at the time of loading system or user programs. Initial Program Loaders are written in machine code (binary form) and are loaded using a bootstrap program.

System Programs
Certain of the system programs (monitors) have the facility to load user programs, in these cases the routines within the system program provide the same functions as the initial program loaders.

INITIAL PROGRAM LOADER

The initial program loader provides the system with the ability to automatically load and run an initial program loader, or similar program, from devices connected to the programmed or an input/output processor channel.

Organization
The option consists of a 64-word ROM mounted on the CPU card, and holding a bootstrap program, and the necessary control circuits to load and run the bootstrap using parameters previously set onto the 16 data switches. The parameters set on the data switches are:

bit

0 1 = IPL loaded from ASR, 4 × 4 format
0 = IPL loaded from other devices

1 1 = IPL loaded from disc
0 = IPL loaded from other devices

2 1 . Not used if bit 0 was 0

3 1 = Programmed Channel
0 = I/O Processor

4 - 7 control information for control unit
TY = 0001 MT = 0010
TK = 0111 DK = 0011

8 1 = multiple device control unit
0 = single device control unit

9 1 if disc in system is used

10 - 15device address of device from which IPL is loaded

Where a device has no specific setting requirements on the data switches, for example Cassette Tape, it is sufficient to set the switches to define; 'Other Devices', the correct channel, and the device address and qualification required for the CIO start command.

Operation
The operation of the initial program loader consists of 4 main steps:

1. The bootstrap is copied from the ROM into the first 64 words of central memory.
2. The contents of the 16 data switches are copied into register A15.
3. The CPU is put into INHIBIT INTERRUPT state.
4. The P register is loaded with zero and the CPU started in run mode.

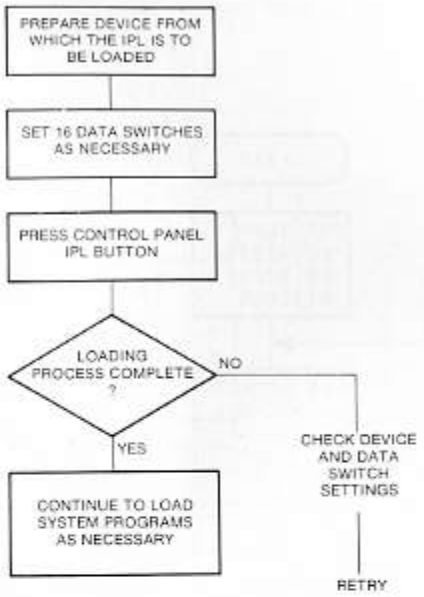


Figure 13.1 Loading the IPL

LOAD MEMORY (FULL CONTROL PANEL)

Figure 13.2 shows the procedure for loading data into memory.

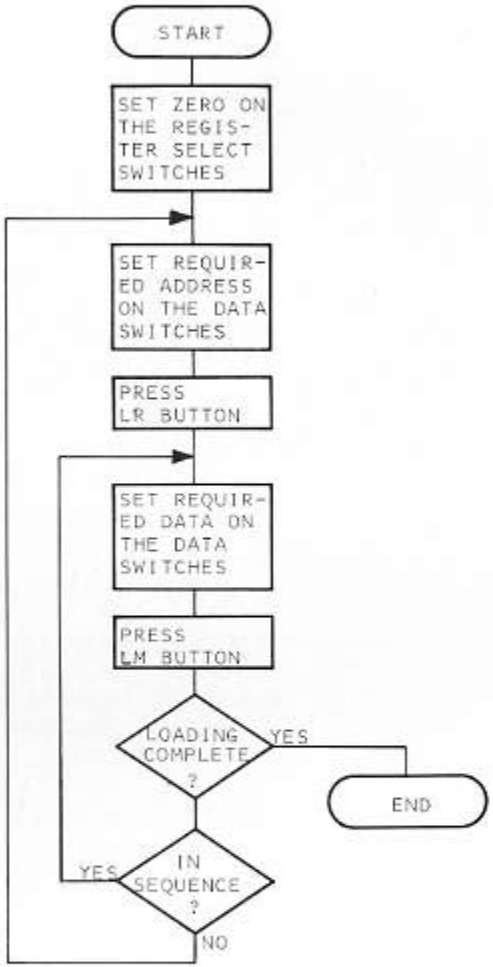


Figure 13.2 Loading Data into Memory

LOAD MEMORY (EXTENDED CONTROL PANEL)

Figure 13.3 shows the procedure for loading data into memory.

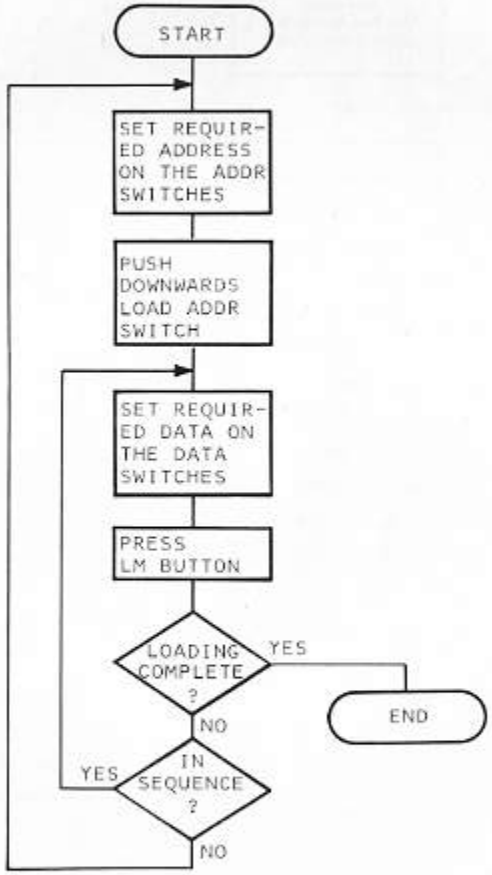


Figure 13.3 Loading Data into Memory

READ MEMORY (FULL CONTROL PANEL)

Figure 13.4 shows the procedure for displaying the contents of memory.

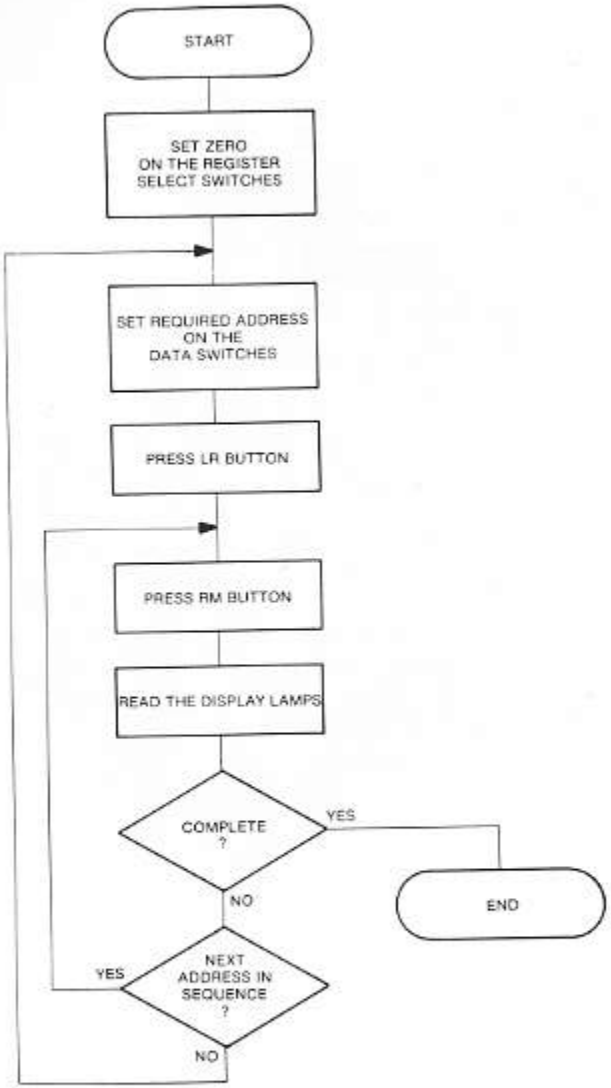


Figure 13.4 Displaying Memory Contents

READ MEMORY (EXTENDED CONTROL PANEL)

Figure 13.5 shows the procedure for displaying the contents of memory.

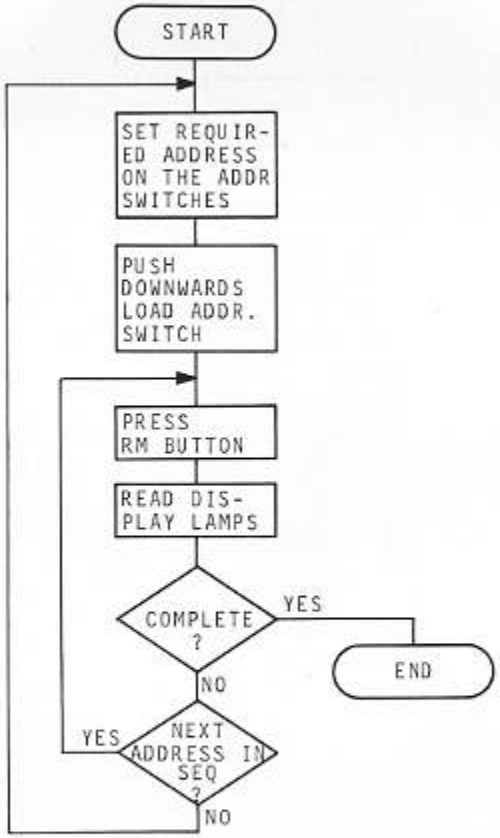


Figure 13.5 Displaying Memory Contents

LOAD REGISTER

Figure 13.6 shows the procedure for loading data into one of the 16 general purpose registers.

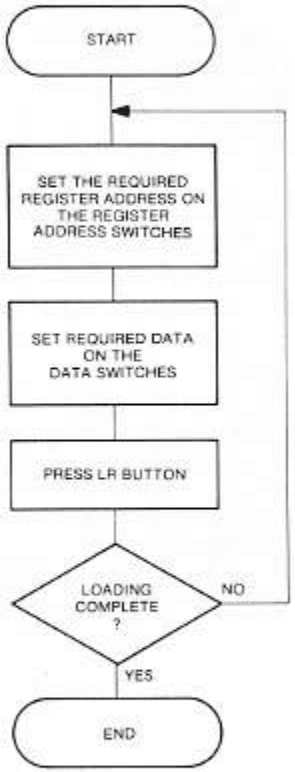


Figure 13.6 Loading Data into Register

READ REGISTER

Figure 13.7 shows the procedure for displaying the contents of one of the 16 general purpose registers. The contents of the program status word may be displayed by pressing the RST button.

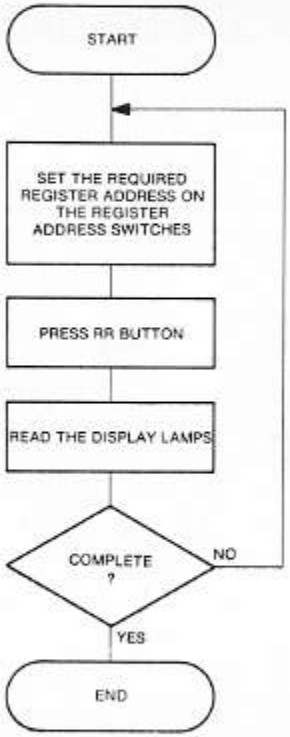


Figure 13.7 Displaying Register Contents

Apart from the main facilities already covered the following additional features are:

1. POWER FAILURE - AUTOMATIC RESTART
2. INTEGRATED V24/V28 SERIAL CONTROL UNIT
3. REAL TIME CLOCK
4. MICRODIAGNOSTICS
5. DETECTION OF PRIVILEGED INSTRUCTIONS

POWER FAILURE - AUTOMATIC RESTART

This facility provides the processor with the ability to terminate processing in an orderly manner after the detection of a power failure, and to restart and resume processing correctly after the restoration of power.

Apart from separate peripherals, all the system's power supplies, whether within the basic cabinet or equipment shelves, are considered necessary for the correct operation of the system. The failure of any of the supplies is therefore able to raise the power failure signal.

Operation

The power failure signal can be connected to any one of the 8 highest priority interrupt levels. When power failure is detected an interrupt is raised and input/output processor exchanges are inhibited, control of the general purpose bus being given to the CPU. Interrupt action takes place and the associated interrupt routine is executed to save the contents of registers, and if necessary specific areas of MOS memory. Core memory is already protected and thus no loss of data from core occurs even if total power failure occurs before completion of the saving routine. On restoration of power the system restarts and CPU operation continues with the restoration of all registers and areas saved before completing the interrupt routine and returning to the originally interrupted program. The power failure interrupt is reset as necessary by the use of the Reset Internal Interrupt (RIT) instruction.

The power failure signal may also be raised at initial power on time if the control panel key switch is set to the LOCK position. In this position the CPU is started and provided the power failure signal is connected to an interrupt level the restoring routine of the level is carried out to restart normal operation at the point it was last suspended.

When the power failure signal is not connected, the CPU will start and remain in the idle state at power on, or after restoration of power following a failure.

Limits
Power failure is set at least 2 ms before the voltage drops below the acceptable limit.

The saving routine should not last more than 2 ms.

Power failure is not set for detected losses of less than 5 ms. The contents of a memory location involved in a memory cycle at the time of total failure is not guaranteed.

REAL TIME CLOCK

A real time clock is available within the system, control of the clock being provided by the control panel key:

ON - RTC stopped
ON RTC - } RTC running
LOCK - }

Once running the RTC generates a signal with reference to the main power supply frequency and is not able to be stopped by program. The generated signal may be connected to any of the 8 highest priority interrupt levels and is thus able to raise an interrupt every 20 ms for 50 cps supplies or 16.67 ms for 60 cps supplies. The associated interrupt must be cleared using the Reset Internal Interrupt (RIT) instruction and the RTC routine may be used as required within the system.
An optional programmable real time clock is available on one board, requiring one slot in the mounting box.

INTEGRATED V24/V28 SERIAL CONTROL UNIT

A V24/V28 Serial Control Unit is available within the system mounted on the CPU board. This control unit allows to attach one of the following asynchronous peripherals as I/O console:

- ASR
- PER3100
- Display

} with V24 interface

The transmission speeds are 110, 600, 1200, 2400, 4800 or 9600 bps.
The speed selection is made by straps on the card. Also selected by straps may be the parity; odd, even or no parity. Odd or even parity is generated or checked by the controller. The number of stop bits, one or two, is also selectable by straps and are generated by the controller.

Organisation
Operation of the control unit is only possible via the programmed channel through the general purpose bus. Connection from the control unit to the peripheral must be according the V24/V28 recommendations.
Data are transferred serially to the control unit and is carried out in parallel by the use of OTR/INR instructions, bits 8 - 15 of a specified register being used.

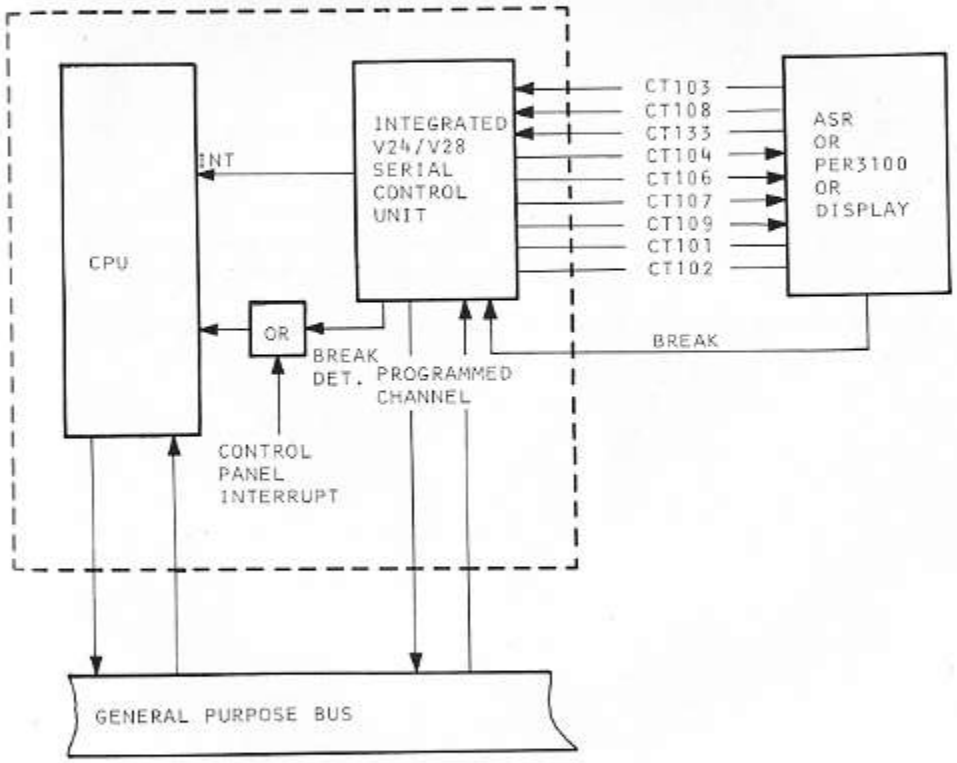


Figure 14.1 Integrated serial control unit

Break feature
Pressing the 'Break' key on the peripheral's keyboard is always accepted by the serial control unit. The activated interrupt is 'ORed' with the Control Panel interrupt.

Operation
The control unit operates in the same manner as other control units, commencing in the inactive state, transferring during the exchange and execute states, and stopping in the wait state. Operation may be in either wait or interrupt mode. Input/output instructions recognizable as commands to the unit are:

CIO	START	input/output
CIO	STOP	
OTR		
INR		
SST		

Responses to these commands are set into the condition register in the normal manner.

The interrupt generated when the control unit is in the exchange or wait states may be connected to any one of the 8 highest interrupt levels and such an interrupt is cleared by the sending of an appropiate I/O command to the unit.

Figures 14.2 and 14.3 show flowcharts of possible methods of programing the V24 controller.

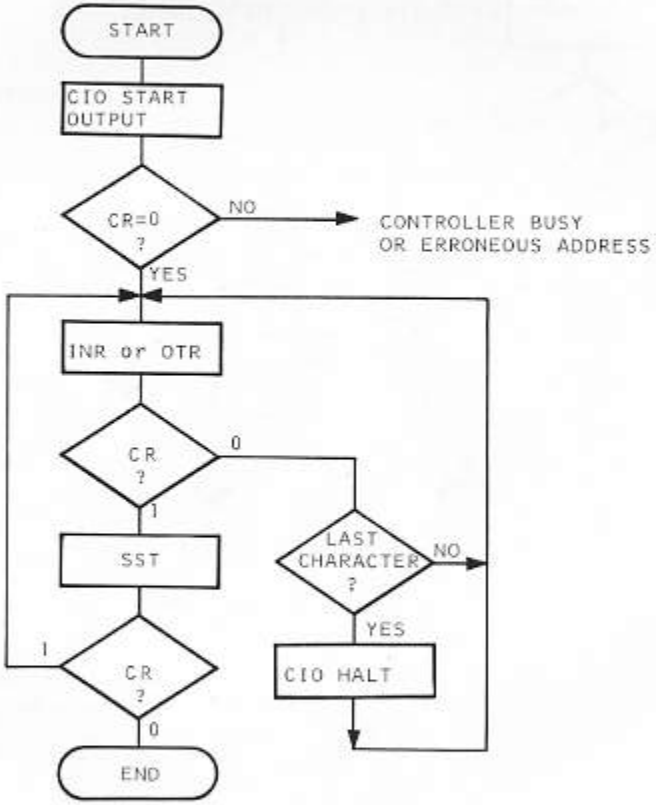


Figure 14.2 Wait mode

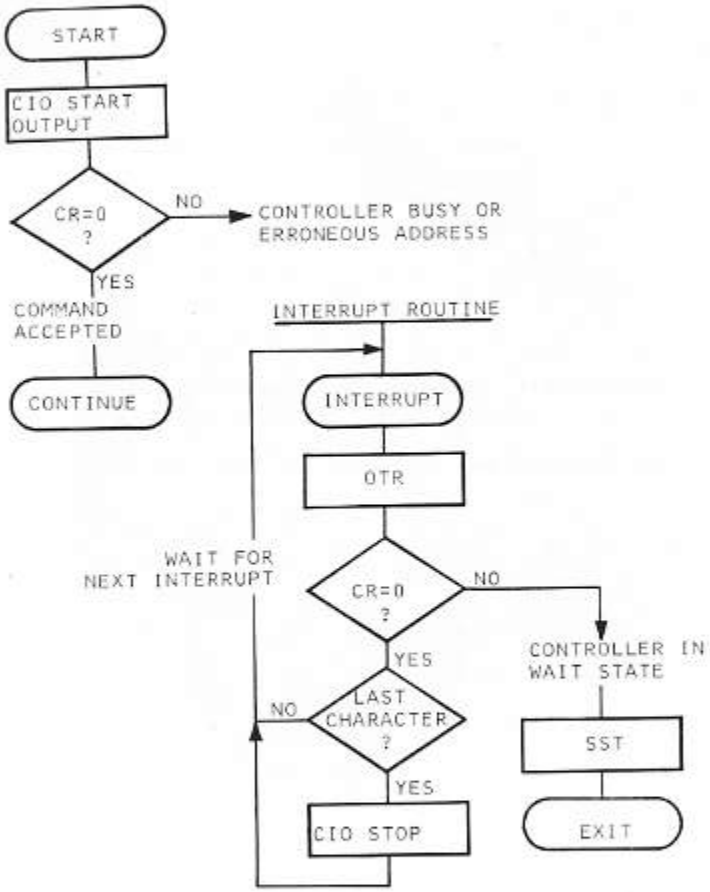


Figure 14.3 Interrupt mode

MICRODIAGNOSTICS

The P856M and the P857M contain an automatic testing feature in the form of a microprogrammed diagnostic built into the CPU logic. Successful running of the tests indicate that sufficient parts of the CPU function for loading of test programs.
The microdiagnostics for the P856M test the first 4k of memory and for the P857M the first 16k of memory. The prerequisite tool is the FULL CONTROL PANEL or the EXTENDED CONTROL PANEL, as the results of the tests are displayed on the data lamps.
About 100 words are reserved for the microdiagnostic program.
The test can only be performed when the key in the key switch is in the TEST position.

Test Procedures
Before starting any test, except for steps A to D included in the Test 2, the user has to set a control unit address on data switches 2 to 7 included to check the dialogue through the Bus between the CPU and the control unit.

Test 1 Automatic Test
This is a fast check which automatically goes through a number of operations. If the tests have been satisfactory special codes are displayed on the data lamps.

- set data switch 0 to 0
- set a control unit address on data switches 2 thru 7
- press RUN button
- wait for display of code no 4
  code 4: data lamp 12 off
  all other lamps lit
  if this code is not displayed go to Test 2
- press LM button and wait for display of code 5
  code 5: all lamps lit
  If the code is not displayed go to Test 2.

Test 2 Step-by-step testing
This sequence may be used if Test 1 showed an erroneous display or if the user wishes to perform separate tests. In these tests the user verifies the operation of the control panel up to the memory.

A. Control Panel test
Each data key and the lamp above it are tested by setting the key in the 'up' position after which the lamp must be lit.
Press LR button to go to the next step.

B. L register test
This step includes the GP BUS and the L register in the test. The operator

may use the switches in the same way as described under control panel. Press LR button to go to the M register test.

C. M register test
This step includes the M register (through the C selector and ALU) in the thest. The operator may use the switches in the same way as described under control panel. Press the LR button to go to the Q register test.

D. Q register test
This step includes the Q register in the test. The operator may use the switches in the same way as described under control panel.

From this moment on the operator may choose among three data path tests, an instruction simulation test or a memory test by setting on the data switches a hexadecimal number and a control unit address, followed by pressing the LR button.
If the relevant test is executed without errors the data lamps display a certain code.

It is possible to skip the visual tests A thru D. The user must then set switch 0 to 0, set a control unit address on switches 2 thru 7, and set switch 15 to 1. Next press the LR button 4 times. Then wait for display of code 1. Press LR button and wait for display of code 2. Press LR button and wait for display of code 3. Press LR (or RUN) button for display of code 4. Press LM (or LR) button for display of code 5.

Test 3 Chained test
In this mode the hardware is tested in a loop which may be stopped by operation of data switch 0.

- set data switch 0 to 1, a control unit address on switches 2 thru 7, and switch 15 to 1.
- press LR button 4 times. The microprogram starts looping.

To stop the loop:
- set switch 0 to 0.
  One of the 5 codes as listed above is displayed. If it is not code 5 press the LR button as many times until code 5 appears.

To restart the loop set switch 0 to 1.
To restart at the beginning of the test turn the key in the key switch to OFF and next to TEST. Set switch 0 to 1, set the control unit address, and set switch 15 to 1 and continue as described above.

	Hexa no on data switches	Test functions	Display on data lamps when no fault is found
data path test	/0001 + CU address	- shift left Q reg. - bus A selection - constant 'TWO' - QO test - A or B, A+B and B inverted ALU functions - ALU = 0	code 1 lamp 15 OFF all other lamps lit
data path test	/0002 + CU address	- shift right Q reg. - ALUZERO - A-B, A+B and crossed A ALU functions - constant 'TEN' - P reg, P - 2 function	code 2 lamp 14 OFF all other lamps lit
data path test	/0004 + CU address	- A operand shifted right - 4 x A function - reading and writing scratch pad	code 3 lamp 13 OFF all other lamps lit
instruction simulation	/0008 + CU address	DLA - K is loaded with DLA code - values loaded in A1 and A2 - branch to DLA micro program - return to microdiagnostic program RB K is loaded - RB microprogram next address generated by PLA	code 4 lamp 12 OFF all other lamps lit
memory test	/0010 + CU address	- bit 15 is set to 1 in all addresses of a 4k/16k block - the block is read and verified - the 1 is shifted left 1 position etc. next: - all words of a 4k/16k block receive their address values as contents these values are verified - tests the TMP-TPM dialogue	code 5 all lamps lit

DETECTION OF PRIVILEGED INSTRUCTIONS

The central processor may operate in two modes:
- system mode
- user mode

System Mode
All available instructions may be executed and the whole memory is accessible. The programmer may use privileged instructions which modify the CPU state namely, the I/O instructions, External transfer instructions and instructions modifying the contents of the stack pointer A15.
The monitor and system programs are executed in this mode.

User mode
User programs operating under monitor control are executed in this mode and any attempt to execute a privileged instruction causes the Trap action to be activated (see page 7-5).
If, however, system allocation is required an LKM instruction sets the CPU, through the monitor, in the system mode.
When the CPU is operating in user mode bit 15 of the PSW is set to 1.

15 Data Communication and Digital Input/Output

Data Communication
A full range of data communication control units for synchronous and asynchronous transmission makes use of the latest LSI technology for increased performance and reliability.
All control units may be plugged in the mounting box or equipment shelf to allow systems to be built easily. A diagnostic box permits the user to verify his system.

The following data communication control units are available:

SLCU2S P847-060	A synchronous double-buffered line control unit which controls one full duplex line or two half duplex lines. It handles 5, 6, 7 or 8 bit characters at a maximum speed of 200,000 bits per second on inplant lines or 20,000 bits per second for outplant lines. The modem interface is V24/V28.
SLCU4 P847-070	A synchronous double-buffered control unit which handles two full duplex lines or four half duplex lines. It recognises 5, 6, 7 or 8 bit characters at a maximum speed of 100,000 bps for inplant lines or 9,600 bps for outplant lines. The modem interface is V24/V28.
AMA8A P845-060	An asynchronous multiplexor for 8 half duplex or 8 full duplex lines. The following speeds are possible: 50, 75, 100, 110, 150, 200, 300, 600, 1200, 2400, 4800 or 9600 bps selectable per line. The control unit recognises 5, 6, 7 or 8 bit characters. The modem interface is V24/V28.
AMA8C P845-070	This control unit is similar to the AMA8A but designed for inplant use. Each line has a four wire current loop interface or a TTL compatible interface.
ALCU2 P846-060	Asynchronous line control unit for handling one full duplex line or two half duplex lines. It recognises 5, 6, 7 or 8 bit characters. The line speed is selectable 300, 600, 1200, 2400, 4800 or 9600 bps.
ALCU4 P846-070	Asynchronous line control unit for handling two full duplex or four half duplex lines. The other features are the same as for the ALCU2.

AMA16 P844-060	A multiplexor for 16 full duplex asynchronous lines, capable of handling the following speeds: 50, 75, 100, 150, or 200 bps. The same speed must be selected for all lines. Characters are assembled under software control. The interface is TTL compatible.
V28CM P844-110	Autocalling Unit Control Module for 32 lines in and 32 lines out. Interface level according to V24/V28 recommandations.
Modem panel (+ optional visualisation panel)	Connects modem and control unit. The visualisation panel shows for which line the 'modem ready' signal is active. The panel may control up to 32 lines.
Diagnostics Box	This box allows to test in an easy manner the control units in a system. Also special test programs are available.

Digital Input/Output System

The Digital Input/Output System (DIOS) is a general purpose system which acts as an interface between the computer and any external equipment. Its function is to control the exchange of 16-bit data words in input as well as output via the programmed channel.
DIOS is delivered on two Dual Input/Output Digital cards (DIOD):

P837-001	one 16-bit word IN one 16-bit word OUT + level adaptor TTL interface	2 external call signals connected to one interrupt level and two response (OK) signals
P837-002	two 16-bit words IN two 16-bit words OUT + level adaptor TTL interface	4 external call signals connected to two interrupt levels and four response (OK) signals

These cards may be plugged in the mounting box or equipment shelf.

Modular I/O System (MIOS)

MIOS is a separate rack mounting system for connecting the system to the General Purpose Bus. The control unit for this system (PC 1207/00 type M5D) handles the basic modular input/output system of up to 16 modules.
MIOS can be configured so as to be almost custom made for any analog/digital application, and can be used for functions such as data acquisition, control analysis, monitoring, and testing in a diversity of environments.

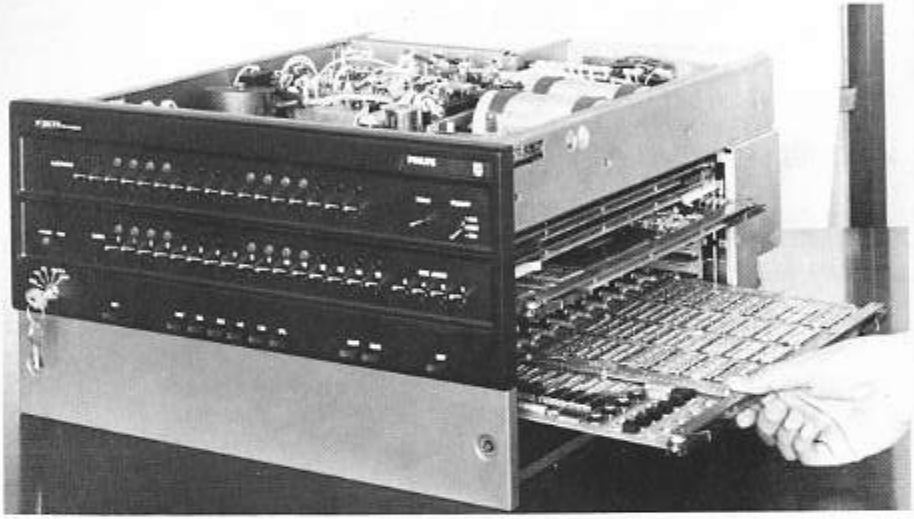
The following modules are available:

D-MODULES

Input:	Digital Input Solid-state Module Digital Input Priority Interrupt Module Digital Input Isolating Module Digital Input Counter Module Time Interval and period Module
Output:	Digital Output Solid-state Module Pulse Output Control Module Analog Output Fast Module Analog Output Control Module

A-MODULES

Analog Scan Control Module
Analog Input Solid-state Module
Analog Input low-level Module
Analog Input high-level Module



P857M in M4M mounting box

CABINETS

The basic cabinets contain standard 19″ racks which are used to hold mounting boxes, equipment shelves and various peripheral equipment. The mounting boxes and equipment shelves are able to contain and provide system d.c. power and cooling to the printed circuit boards fitted within them. Each mounting box has dedicated locations for the fitting of the processor cards and the first memory module. Figure 16.2 shows the possible layout of equipment within the cabinet and includes:

Central Processing Unit
Paper Tape Reader
Paper Tape Punch
Cassette Tape Units
Moving Head Disc Units.

BASIC MOUNTING BOX AND EQUIPMENT SHELVES

M1 Mounting Box (for up to 16k P856M)

Number of slots	4 sub-assembly slots for cards connected directly to the GP Bus.
Size	Height 3U (approx. 132.5 mm), depth 585 mm.
Power Supply	+5 V 15A –5V 0.8A +16V 4.5A ±18V unregulated, 1A

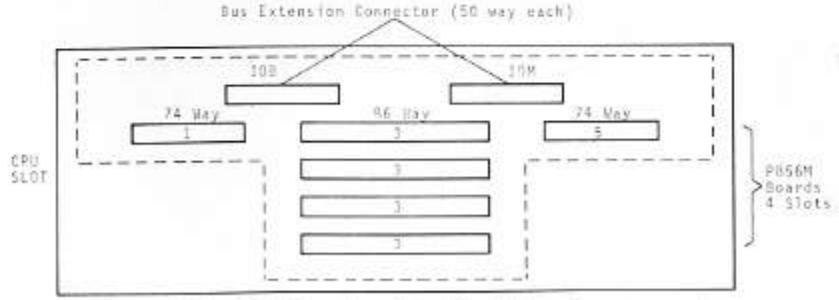


Figure 16.1 M1 Mounting Box Backplane Arrangement

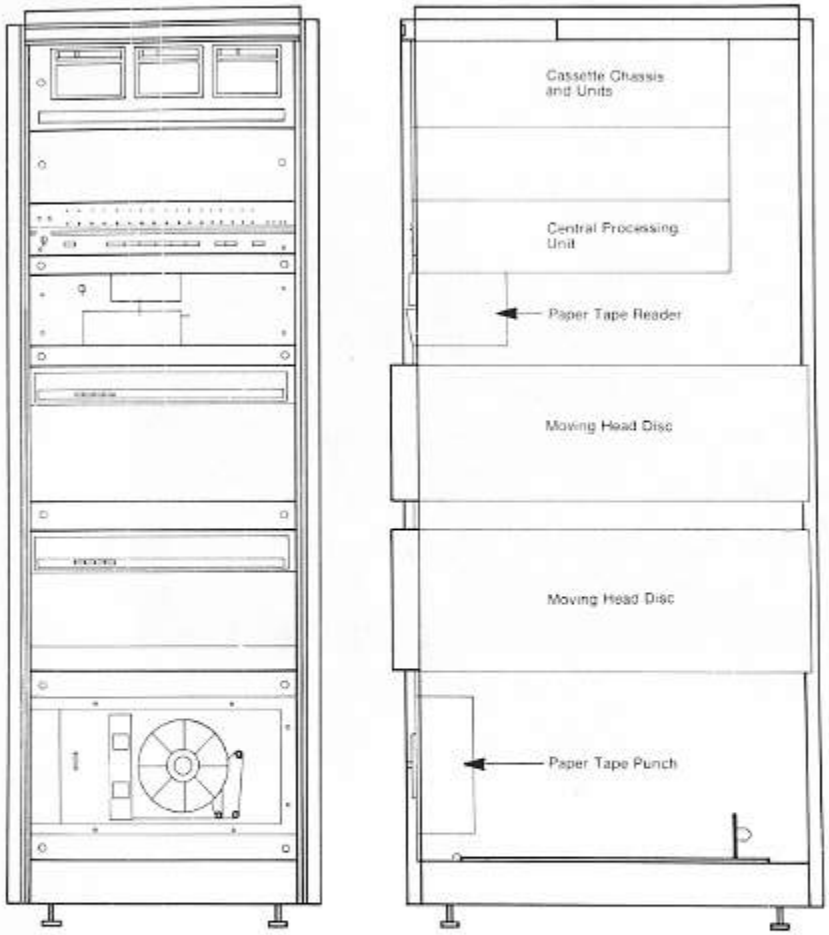


Figure 16.2 Example of Equipment Mounted in a Cabinet

M4 Mounting Box (for up to 32k P856M)

Number of Slots : 10 sub-assembly slots for cards directly connected to the GP Bus.

Size : Height 6 U (approx. 265 mm), depth 550 mm.

Power Supply : +5V, 43A
−5V, 1.6A
+16V, 8.5A
±18V, unregulated, 2A

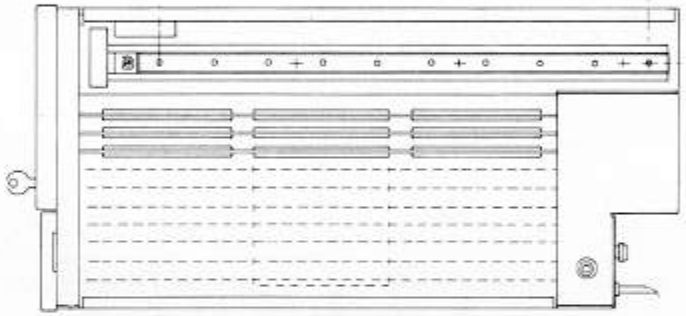


Figure 16.3 M4 Mounting Box Side View

M4M Mounting Box (for up to 64k P857M)
This is the same mounting box as the M4 mounting box but contains extra wiring for the MMU board.The CPU must be plugged in the first slot, the MMU in the second and the FPP in the third slot.

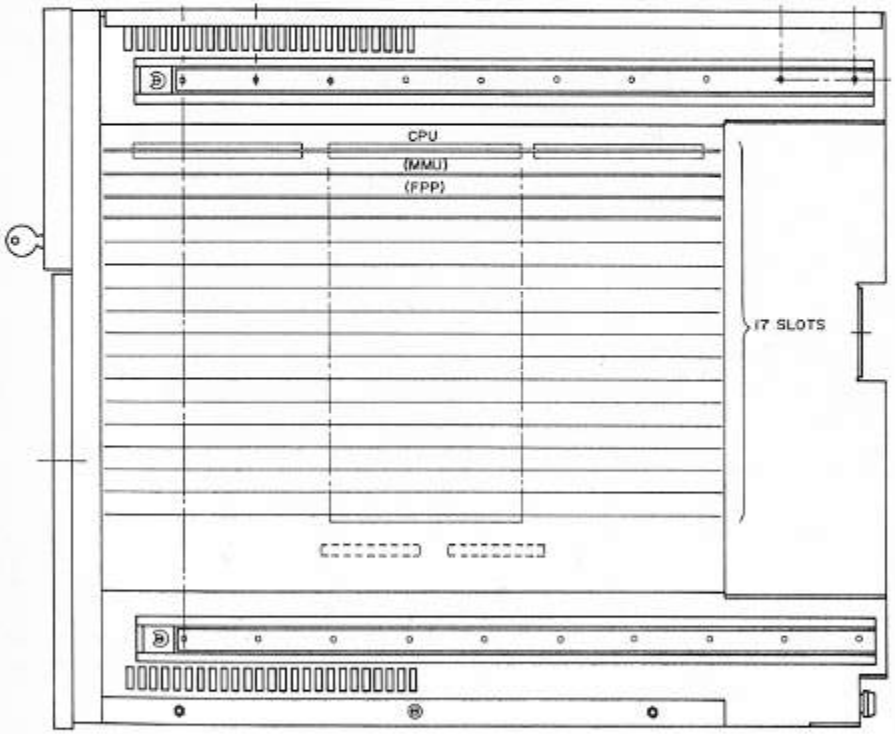
M5M Mounting Box (for up to 128k P857M)

Number of Slots : 17 sub-assembly slots for cards directly connected to the GP Bus.

Size : Height 11 U (approx. 489 mm), depth 550 mm.

Power supply : +5V, 86A
−5V, 4A
+16V, 17A
±18V, unregulated, 4 A.

For power consumption reasons it is advised not to plug more than 4 memory modules in 4 of the first 10 slots. Other memory modules may be plugged into slots 11 thru 17.



Equipment Shelf P843-001

Number of Slots : 6 sub-assembly slots for control units connected directly to the GP Bus.

Size : Height 3U (approx. 132.5 mm).

Power Supply : +5V 18A
+18 V 2A
-18V 2A

Other Facilities Where the Equipment Shelf is situated at the end of the GP Bus a termination is necessary. The Bus can be terminated by the inclusion within the shelf, of the required termination boards.

Interconnection between units

The interconnection between units is carried out via the backplane wiring within the mounting box and the equipment shelves and by the use of signal cables between the control units and devices. Interconnection between the mounting box and equipment shelf is carried out by the GP Bus and Break Line cables. GP Bus and Break Line cable connectors being fitted on the backplane of the mounting box and equipment shelf. Where necessary it is also possible to extend the GP Bus and Break Line cables to self contained control units.

INSTALLATION

All the standard units of the system have been designed for straight forward installation, and in most cases very few or no special considerations will be necessary, either with reference to the layout of the equipment, or to the installation site itself. However, because of the flexibility, and therefore widely differing possibilities for system configuration, each site must be planned and installed with reference to its own configuration. The detailed information required for any installation may be found in the Installation Manual and associated publications dealing with the peripheral devices to be used.

Electrical Supplies

Systems are supplied for connection to a mains supply which should be wired for the use of the system only. The supply requirements are:

System 3 wire: single phase, neutral and earth, or two phases and earth.

Voltage 100V, 115V, 220V or 240V ± 10%. Standard is 220V.

Frequency 50 ± 2 Hz or 60 ± 3 Hz.

Power — The supply circuit should be designed to adequately meet the current requirements of the system, and where expansion is envisaged sufficient capacity to meet the expansion should be provided at the time of initial installation to avoid major power re-organization.

Environmental Control

The requirement for environmental control will depend entirely on the configuration and siting of the system and may vary from a normal office environment for the smaller non-magnetic orientated systems to full air conditioning for sophisticated magnetic systems.

The general operating conditions normally accepted within the computer room are listed below but in all cases the requirements of any of the equipment within the system, which is not within these tolerances, must be met.

Temperature	- 0°C to +45°C.
Relative Humidity	- up to 90% without condensation.

Safety

The individual units which comprise a standard system have been designed to meet necessary safety standards. Safety precautions for non-standard units and the system as an installation will depend on local regulations and conditions, and should be designed to adequately cover the initial installation and any future planned expansion.

INTERFACING

As all interfacing between the units of the system is carried out via the general purpose bus, the design of peripheral control units, whether for standard or non-standard devices, is made easier. Interfacing circuits within control units are designed to the same specification, and as timing is carried out within the bus circuitry on a signal and response basis, then timing control circuits within control units may be reduced. Control units for connection directly to the GP Bus and for controlling basic peripherals are available, in certain configurations, combined on one multiple control unit board, whilst control units for the more sophisticated magnetic peripherals are available on separate boards.
Complete details of all interfacing requirements may be found in the Interface Manual, which should be used whenever exact references are required.