CIO *Control Input/Output* **CIO**

P851M
P852M
P856M
P857M

Syntax: [label] ␣ CIO ␣ r3, {0 / 1}, dev

This instruction permits to start or to stop an I/O operation on a peripheral device, depending whether bit 9 is set (start) or reset (stop).
During the execution of this instruction the contents of bit 10–15 are sent, via the bus, to the control unit addressed, together with the contents of the register r3, which contains additional information for the control unit. A survey of the information which may be given in r3 for each control unit is given on the following pages.
A start an I/O operation command is not accepted if the address specified is unknown or if the corresponding device is busy. The stop a data transfer command is always accepted.

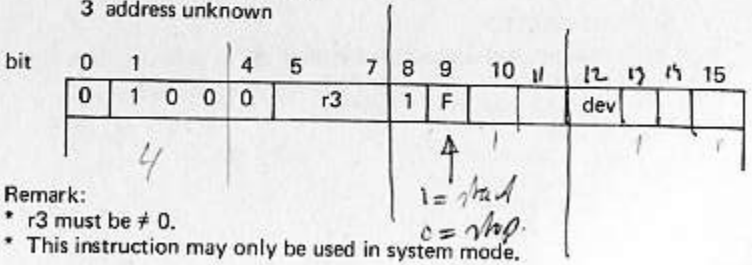
Example:

```
Start an input operation:   LDK     A1,1
                            CIO     A1,1,/10    start input on teletype
                            RB(NA)  *–2         wait until accepted
Start an output operation:  LDK     A1,0
                            CIO     A1,1,/10    start output on teletype
                            RB(NA)  *–2         wait until accepted
Stop the I/O operation:     CIO     A1,0,/10
```

Type	*Syntax*	
T8	CIO r3, 1, address	start input or output
T8	CIO r3, 0, address	stop I/O

Condition register:

CR = 0 command accepted
1 command not accepted
3 address unknown



Remark:
* r3 must be ≠ 0.
* This instruction may only be used in system mode.

Information which must be given in r3 and in the CIO instruction, if required:

ASR

bit 15 = 1 input
0 output

PUNCHED TAPE READER

r3 not significant

TAPE PUNCH

r3 not significant

SERIAL CU

CIO READ

bit 10 = 1 echo mode
0 no echo mode

bit 13 14
1 1 7 data bits + parity bit (odd)
1 0 7 data bits + parity bit (even)
0 1 7 data bits, no parity
0 0 8 data bits

bit 15 = 1

CIO WRITE

bit 13 14 see CIO READ

bit 15 = 0

CARD READER

r3 not significant

LINE PRINTER

r3 not significant

CASSETTE

In CIO instruction must be specified:
bit 10,11 drive no
bits 12 thru 15 address

In r3:

bit 12	13	14	15	
0	0	0	0	unlock
0	0	0	1	erase
0	0	1	0	backspace
0	1	0	1	write a block forward
0	1	1	1	read a block forward
1	0	0	0	rewind
1	0	0	1	write tape mark
1	0	1	0	search tape mark backward
1	0	1	1	search tape mark forward

DK1215

In CIO instruction must be specified:
bit 10,11 disk no
bit 12 thru 15 address

In r3:

CIO SEEK

bit 4 thru 12 cylinder no. $0 \leq N \leq 203$

bit 14 = 1
bit 15 = 0

CIO SEEK TO ZERO

bit 14 = 1
bit 15 = 1

CIO WRITE A SECTOR

bit 9 thru 13 sector address from 0 to 31

bit 14 = 0
bit 15 = 1

CIO READ A SECTOR

bit 9 thru 13 sector address from 0 to 31

bit 14 = 0
bit 15 = 0

PROGRAMM. REAL TIME CLOCK

r3 specifies the interrupt rate selection

bit 0 = 0

bit 15 = 1 1 millisecond
bit 14 = 1 5 milliseconds
bit 13 = 1 10 milliseconds
bit 12 = 1 20 milliseconds

bit 0 = 1

bit 1 thru 15 the number of milliseconds

MAGNETIC TAPE

bit 10	11	12	13	14	15	
0	0	0	0	1	1	write
0	1	0	0	0	1	write file mark
0	1	1	0	0	1	erase gap
0	0	1	0	1	0	read one block
0	0	0	0	1	0	read with check characters
0	0	x	0	0	0	forward space block
0	0	x	1	0	0	backward space block
0	1	x	0	0	0	search file mark forward
0	1	x	1	0	0	search file mark backward
1	x	x	1	x	x	rewind
1	x	x	0	x	x	off line
1	x	1	1	x	x	load and on line (for 1600BPI)

(x = not significant)

SERIAL CU P851M

bit 12	13	
x	0	no parity
0	1	even parity
1	1	odd parity

bit 15 =		
0		output
1		input

SALCU

bit 11 =		
0		without echo
1		with echo

bit 12	13	
x	0	no parity
0	1	even parity
1	1	odd parity

Input is always on even address.
Output is always on input address + 1.

HDLC

CIO Start input

bit 12	13	14	15	
x	0	0	1	disconnect modem
x	0	1	0	connect modem
x	0	1	1	wait for call
0	1	0	1	receive data (prog. chan)
0	1	0	0	alarm receive data (prog. chan)
1	1	0	1	receive data (I/O proc)
1	1	0	0	alarm receive data (I/O proc)

CIO Start output

bit 4	5	6	7	12	13	14	15	
no. of true data				0	0	1	0	transmit 4 wire (Prog. Chan)
bits. If zero, the				0	0	1	1	transmit 2 wire (Prog. Chan)
length of last word				1	0	1	0	transmit 4 wire (I/O Proc)
to be sent is 16 bits				1	0	1	1	transmit 2 wire (I/O Proc)
not sign.					1	0	0	idle "1"
not sign.					0	0	1	no "request to send"

FLOPPY DISK

In CIO instruction must be specified:

bit 10,11	drive number
bit 12 thru 15	control unit address

The r3 contents must be:

WRITE

bit 0, 1	n+1 records will be written successively
bit 2 thru 12	record number (from 0 to 2001)
bit 13 14 15	
0 0 1	

WRITE AND VERIFY

bit 0 thru 12	see WRITE
bit 13 14 15	
1 0 1	

WRITE WITH DELETED DATA ADDRESS MARKS

bit 0 thru 12	see WRITE
bit 13 14 15	
0 1 0	

WRITE WITH DELETED ADDRESS MARKS AND VERIFY

bit 0 thru 12	see WRITE
bit 13 14 15	
1 1 0	

READ

bit 0 thru 12	see WRITE
bit 13 14 15	
0 0 0	

SEARCH KEY

bit 0 thru 4	0
bit 5 thru 12	number of 8-bit characters of the key number = 1 to 128
bit 13 = 1	search with mask
0	search without mask
bit 14 15	
1 1	

READ RECORD WITH KEY

bit 0 thru 12 0
bit 13 14 15
1 0 0

DOOR LOCK

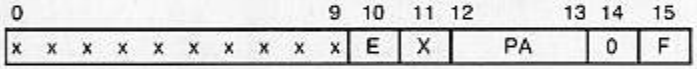
bit 0 thru 10 0
bit 11 12 13 14 15
1 0 1 0 0

DOOR UNLOCK

bit 0 thru 10 0
bit 11 12 13 14 15
0 1 1 0 0

Input/output Instructions for Integrated Serial Control Unit

In I/O instructions for the P858M/P859M integrated serial control unit, the following parameter values apply:
- device address for the integrated serial control unit is /10
- the contents of 'r3' in a CIO Start instruction must be:



X = : not significant
E : 0 = no echo mode — not significant
1 = echo mode — if bit 15 = 0
PA : 00 = no parity
01 = even parity
11 = odd parity
F : 0 = output
1 = input

INR *Input to register* **INR**

P851M
P852M
P856M
P857M

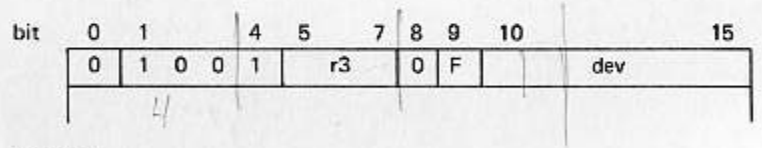
Syntax: [label] ␣ INR ␣ r3, $\left[\begin{smallmatrix}0\\1\end{smallmatrix}\right]$, dev

This instruction allows to transfer one word or character from a device to the register specified in r3.
When a character is transferred the 8 bits are stored in bits 8–15 of register r3 and bits 0–7 are reset to zero.
When a word is transferred all 16 bits of the register r3 are significant.
Bit 9 may be used to give a particular input function which depends on the peripheral used.
This instruction is accepted when the device control unit is in the exchange state. If not accepted the contents of the register are destroyed.

Note: On certain peripherals, e.g. teletype, an ASCII character may or may not be accompanied with a parity bit, depending on the parity chosen. This parity bit can be found in bit 8 of the register r3. When this bit is not systematically reset to zero, e.g. with ANK r3,/7F, the information in memory may be different from the ASCII pattern expected.

Type	*Syntax*	
T8	INR r3, 0, address	
	INR r3, 1, address	depending on control unit

Condition register:
CR = 0 command accepted
1 command not accepted
3 device address unknown



Remark:
* r3 ≠ 0.
* This instruction may only be used in system mode.

OTR	*Output from register*	OTR	P851M P852M P856M P857M

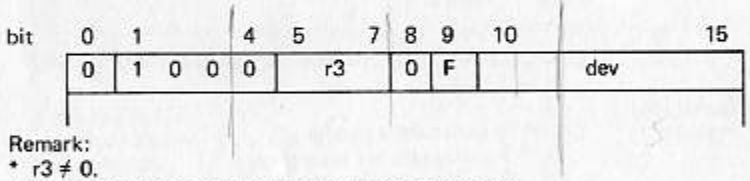
Syntax: [label] ␣ OTR ␣ r3, {0 / 1}, dev

When this instruction is accepted, only if the device control unit is in the exchange state, a data word or character is sent from the register specified by r3 to the peripheral device with address dev. During execution "F" and dev fields are sent to the device via the GP bus. Bit 9 (F) may be used to specify a particular output function which depends on the type of peripheral used.

Type	*Syntax*	
T8	OTR r3, 0, address	
	OTR r3, 1, address	depending on control unit

Condition register:

CR = 0 command accepted
1 command not accepted
3 device address unknown



Remark:
* r3 ≠ 0.
* This instruction may only be used in system mode.

SST	*Send status*	SST	P851M P852M P856M P857M

Syntax: [label] ␣ SST ␣ r3, dev

This instruction is used to know the status of the control unit addressed and should be programmed after an I/O sequence e.g. after CIO STOP.
The instruction is accepted when the control unit addressed is in the Wait State, after which a status word is sent to the register r3.
The following conditions are indicated by fixed bit positions (if significant for the control unit concerned) : see following pages.

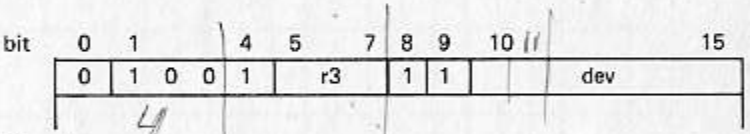
After a not accepted SST instruction the contents of r3 is not significant.

Note: For the programmable real time clock the SST is not significant.

Type	*Syntax*
T8	SST r3, address

Condition register:

CR = 0 command accepted
1 command not accepted
3 device address unknown



Remark:
* r3 must be ≠ 0.
* Address must be ≠ 0.
* This instruction may only be used in system mode.

CU status configuration:

Bit	Description	ASR	PTR	PTP	S.CU	CR	LP	CAS	MT	DK1215	DK40MB	DKFL	SCUZ	SALCU	HDLC
15	Not operable	x	x	x	x	x	x	x	x	x	x	x		x	x
14	Throughput error	x	x		x in	x		x	x	x	x			x	x
13	Parity error				x			x			x		x	x	
	Data fault								x	x		x			
	FCS error														x
12	Incorrect length					x		x	x	x	x	x			x
11	'Break detection'				x										
	Program error							x	x	x		x			
10	End of tape		x					x	x						
	Tape low			x											
	End of reception				x										
	Hopp./Stack. empty/full					x									
	End of carr. detection													x	x
	Retry											x			
9	Calling indicator													x	x
	Dev/tape/drive no.							x	x	x	x	x			
8	Dev/tape/drive no.							x	x	x		x			
	Device ready				x										
	Break detection												x	x	
7	1=A side/0=B side							x							
	4–7 No. of true data bits														x
6	Write protected							x	x			x			
	Seek error									x	x				
	4–7 No. of true data bits														x

1.146

CU status configuration (contd):

Bit	Description	ASR	PTR	PTP	S.CU	CR	LP	CAS	MT	DK1215	DK40MB	DKFL	SCUZ	SALCU	HDLC
	Begin of tape/load point							x	x						
5	Seek completed									x					
	4–7 No. of true data bits														x
	Record not found							x			x	x			
4	Del. data addr. mark											x			
	4–7 No. of true data bits														x
3	Tape mark detection							x							
	File mark detection								x						
	Idle detect														x
2	Rewind								x						
	Abort detect														x
	Flag bad data track										x				
	Key not found											x			
1	Unit rdy after not rdy							x	x	x	x	x			
0															

1.147

TST	*Test status*	TST	P851M P852M P856M P857M

Syntax: [label]␣ TST ␣ r3, dev

This instruction may be used before starting an I/O operation to test whether the control unit addressed is busy. The instruction is always accepted. During the execution of the TST instruction a status word is sent from the control unit to register r3.
A 1 bit is set in bit 15 of the status word sent (busy) for the following control units:

ASR
PUNCHED TAPE READER
TAPE PUNCH
SERIAL CONTROL UNIT P852, P856, P857M
CARD READER
LINE PRINTER
CASSETTE
MAGNETIC TAPE
DK1215
DK40MB
DKFLOPPY
PROG. REAL TIME CLOCK

For some control units additional information may be expected in the status word:

MAGNETIC TAPE: bit 14 = 1 tape transport ready (for 1600 BSI)

PROG. REAL TIME CLOCK: bit 14 = 1 previous command accepted. This bit may be forced to zero.

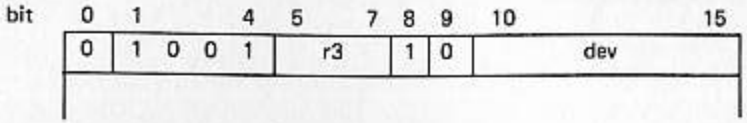
DK40MB: bit 14 = least significant bit of the total record length
bit 1 = most significant bit of the total record length
bit 0 = 0

Note: The serial control unit P851M, the HDLC control unit and SALCU return no significant information when a TST instruction is sent.

Type	*Syntax*
T8	TST r3, address

Condition register:

CR = 0 accepted
3 device address unknown



Remark:
* r3 must be ≠ 0.
* This instruction may only be used in system mode.